

ZZZ1
PCB
D0DAZ@

ZZZ3
LA-6091P
D0DA@

ZZZ4
LS-6094P
D0DA@

ZZZ5
LS-6095P
D0DA@

PJP1
45@DCIN
DC301008S00

ZZZ2
PCB
E0DAZ@

ZZZ6
LA-6091P
E0DA@

ZZZ8
LS-6096P
E0DA@

ZZZ7
LS-6097P
E0DA@

ZZZ9
LS-6098P
E0DA@

ZZZ10
LS-6099P
E0DA@

Compal Confidential

NAVD0 Schematics Document

Intel Pineview Processor with Tigerpoint + DDRII + NV OPTIMUS

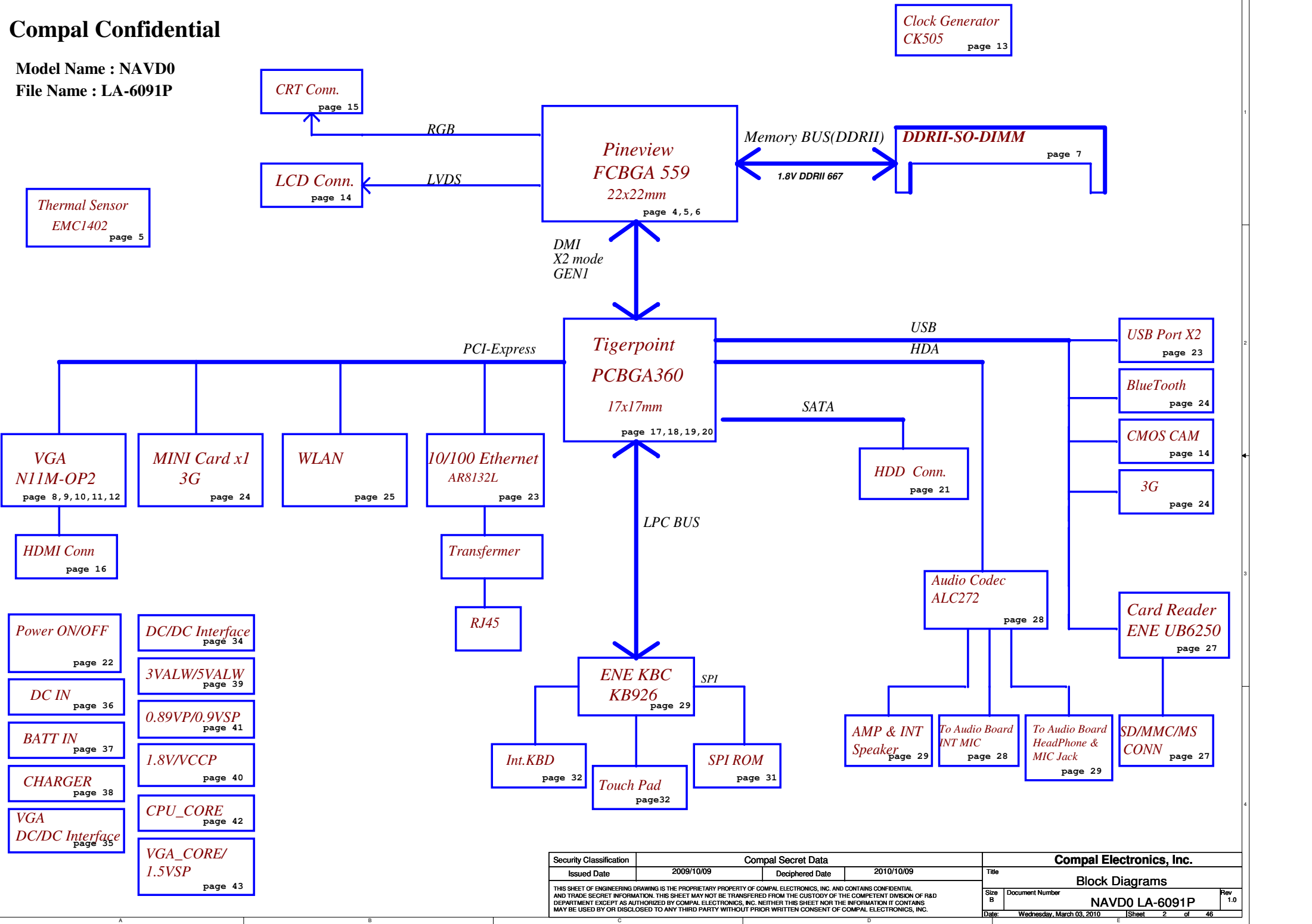
2010-02-09

REV: 1.0

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Model Name : NAVD0
File Name : LA-6091P



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+VCCP	VCCP switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+0.89VS	Graphic core power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table(Page 31)

	VCC	3.3V					
	Ra	100K					
	ID	BRD ID	Rb	Vab-Min	Vab-Typ	Vab-Max	
NAVD0	0	R01 (EVT)	0	0V	0V	0V	
	1	R02 (DVT)	8.2K	0.216V	0.250V	0.289V	
	2	R03 (PVT)	18K	0.436V	0.503V	0.538V	
	3	R10A (MP)	33K	0.712V	0.819V	0.875V	
NAVE0	4	R01 (EVT)	56K	1.036V	1.185V	1.264V	
	5	R02 (DVT)	100K	1.453V	1.650V	1.759V	
	6	R03 (PVT)	200K	1.935V	2.200V	2.341V	
	7	R10A (MP)	NC	2.500V	3.3V	3.3V	

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
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No PCI Device

EC SM Bus1 address

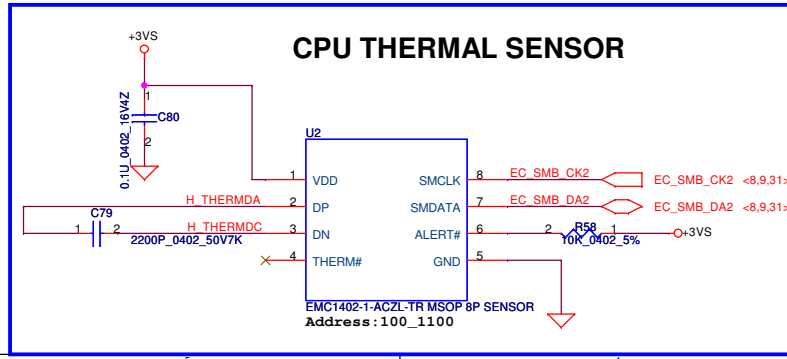
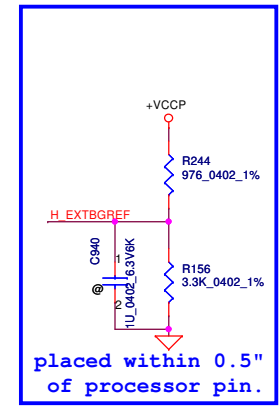
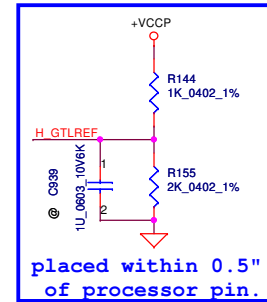
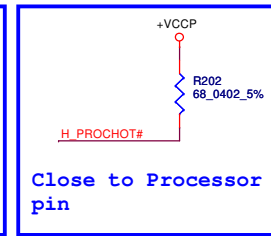
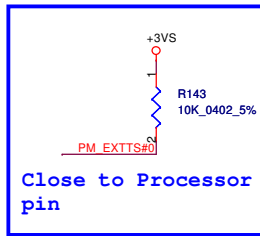
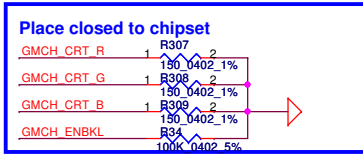
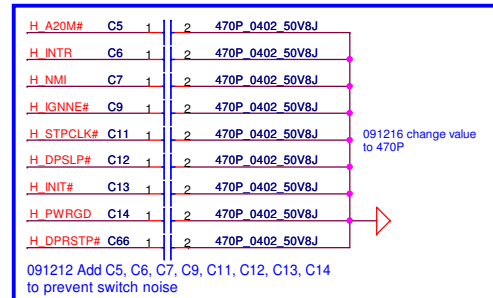
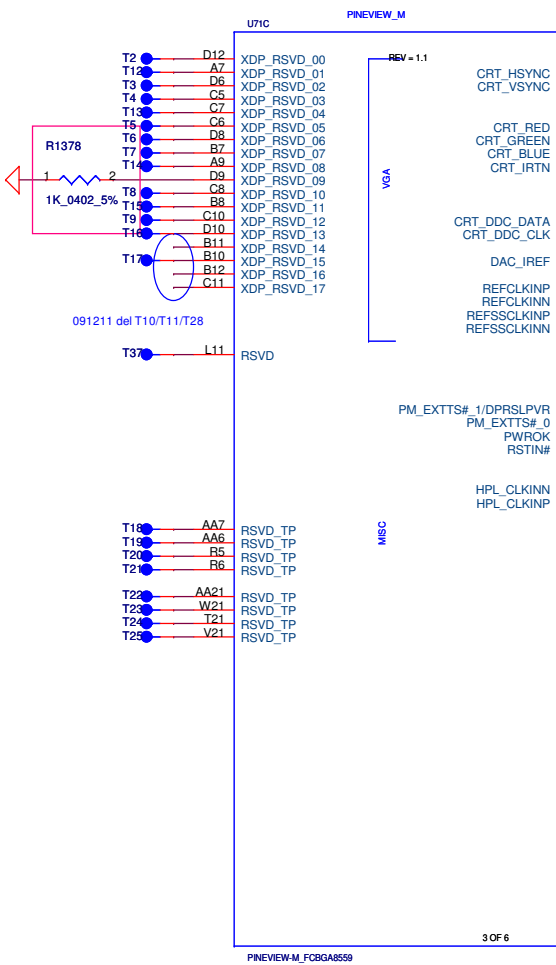
EC SM Bus2 address

Device	Address	Device	Address
Smart Battery	0001 011X b	EMC1402	100_1100

ICH7M SM Bus address

Device	Address
Clock Generator (SLG8SP556VTR)	1101 001Xb
DDR DIMMA	1010 000Xb

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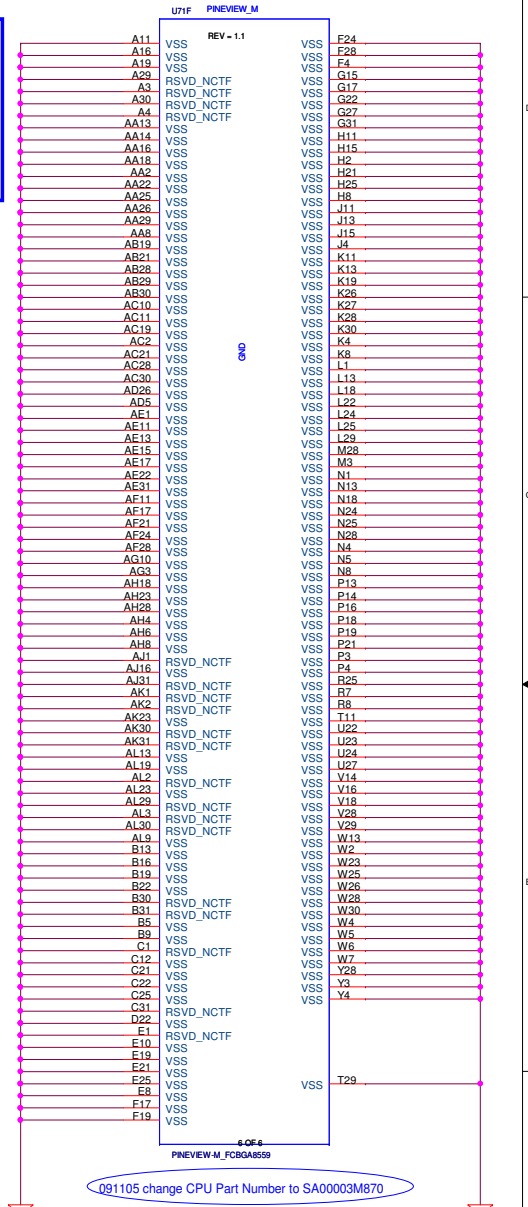
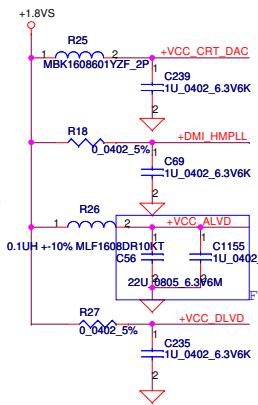
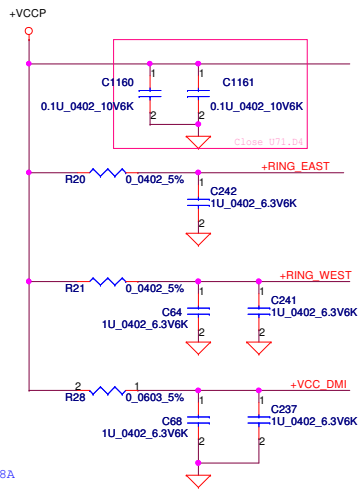
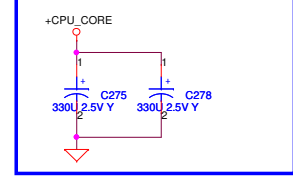
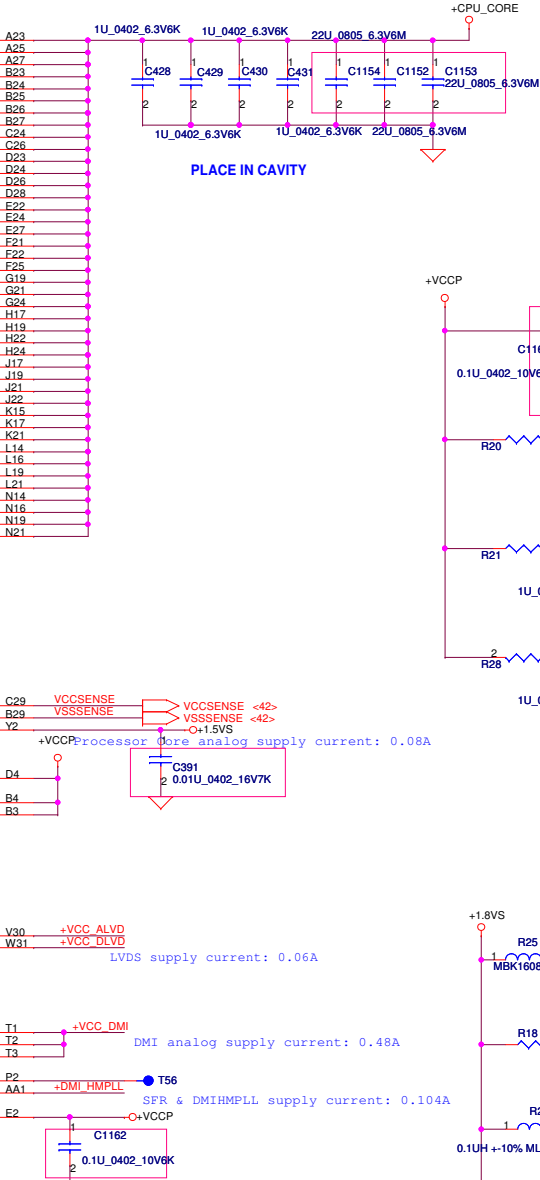
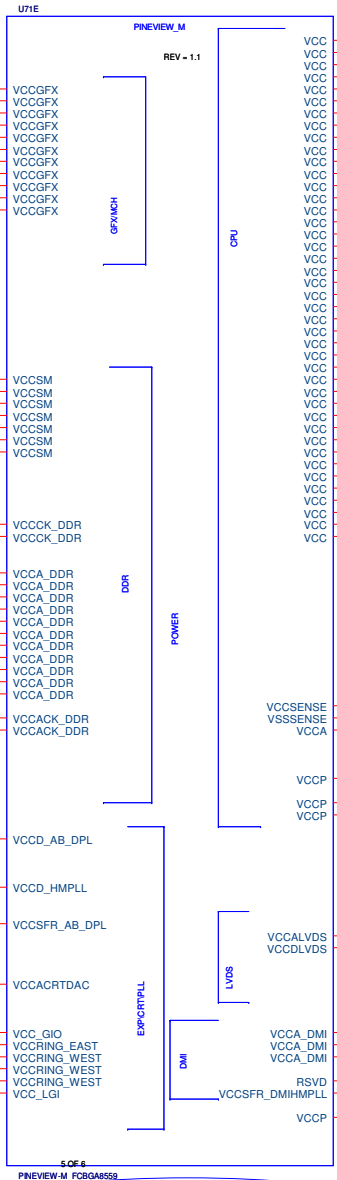
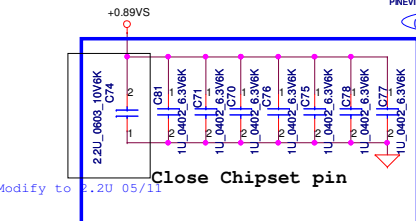
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GFX supply current: 1.38A
Sustained GFX supply current: 1.05A

DDR supply current 2.27A

Display PLL SFR and CRT DAC supply current: 0.154A

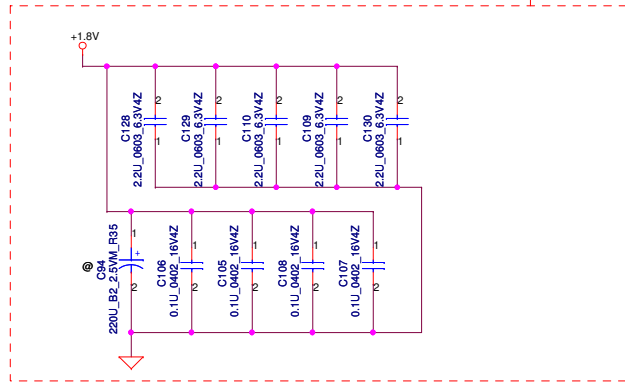
DAC, GIO, LVDS, & LGIO, DPLL, HMPLL supply current: 0.33A



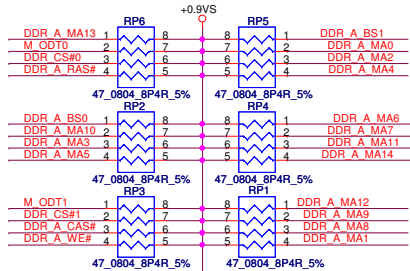
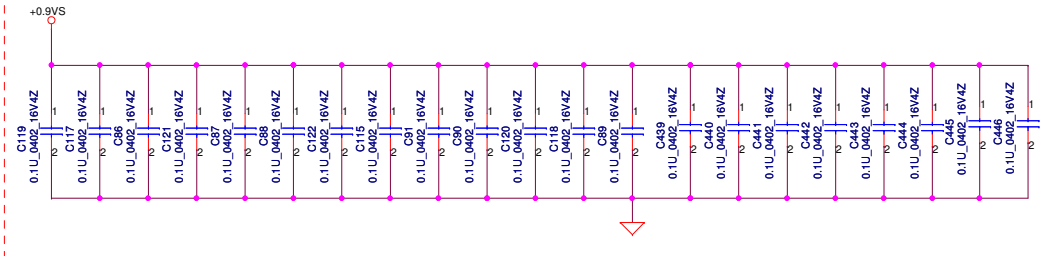
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Deciphered Date				2010/10/09				NAVD0 LA-6091P			
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<4> DDR_A_DQS#[0..7]
<4> DDR_A_D[0..63]
<4> DDR_A_DM[0..7]
<4> DDR_A_DQS[0..7]
<4> DDR_A_MA[0..14]

Layout Note:
Place near JDIM1

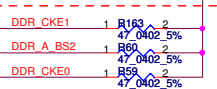


Layout Note:
Place one cap close to every 2 pullup
resistors terminated to +0.9VS

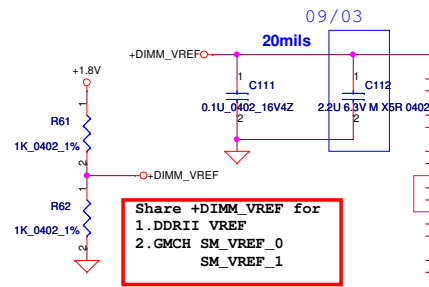


Layout Note:
Place these resistor
closely DIMMA, all
trace length < 750 mll

091204 swap nets for layout



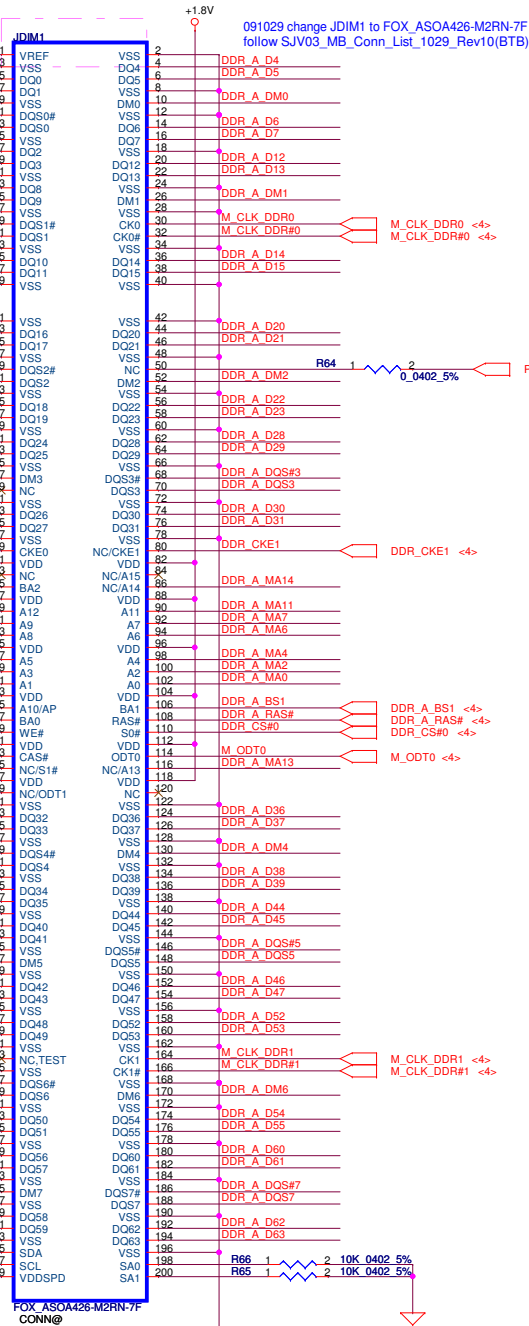
Layout Note:
Place these resistor
closely DIMMA, all
trace length
Max=1.3"



Share +DIMM_VREF for
1.DDRII VREF
2.GMCH SM_VREF_0
SM_VREF_1

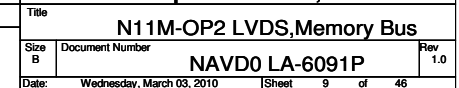
<4> DDR_CKE0
<4> DDR_A_BS2
<4> DDR_A_BS0
<4> DDR_A_WE#
<4> DDR_A_CAS#
<4> DDR_CS#1
<4> M_ODT1

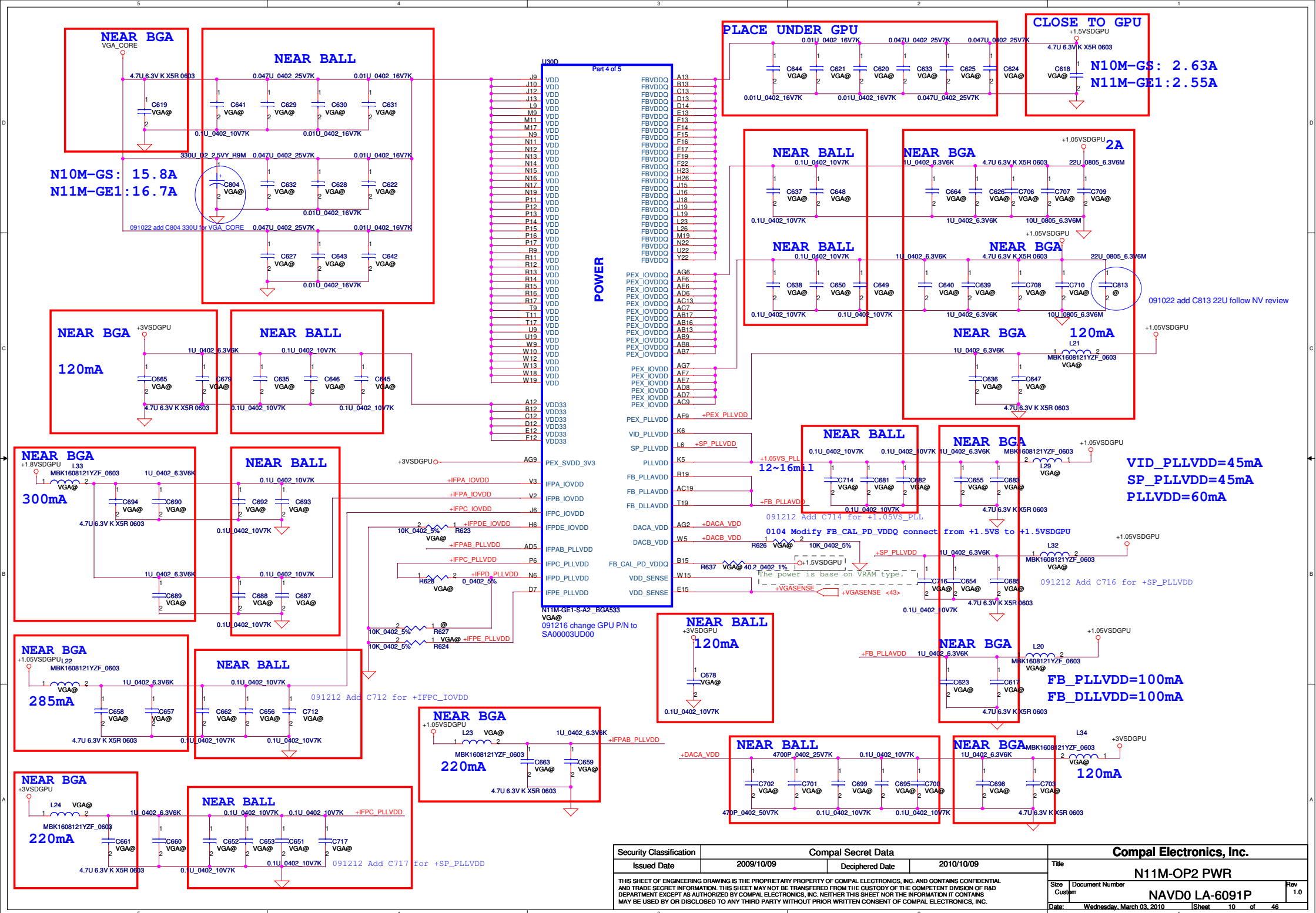
DDR_A D0
DDR_A D1
DDR_A DQS#0
DDR_A DQS0
DDR_A D2
DDR_A D3
DDR_A D8
DDR_A D9
DDR_A DQS#1
DDR_A DQS1
DDR_A D10
DDR_A D11
DDR_A D16
DDR_A D17
DDR_A DQS#2
DDR_A DQS2
DDR_A D18
DDR_A D19
DDR_A D24
DDR_A D25
DDR_A DM3
DDR_A D26
DDR_A D27
DDR_CKE0
DDR_A_BS2
DDR_A_MA12
DDR_A_MA9
DDR_A_MA8
DDR_A_MA5
DDR_A_MA3
DDR_A_MA1
DDR_A_MA10
DDR_A_BS0
DDR_A_WE#
DDR_A_CAS#
DDR_CS#1
M_ODT1
DDR_A D32
DDR_A D33
DDR_A DQS#4
DDR_A DQS4
DDR_A D34
DDR_A D35
DDR_A D40
DDR_A D41
DDR_A DM5
DDR_A D42
DDR_A D43
DDR_A D48
DDR_A D49
DDR_A DQS#6
DDR_A DQS6
DDR_A D50
DDR_A D51
DDR_A D56
DDR_A D57
DDR_A DM7
DDR_A D58
DDR_A D59
CLK_SMBDATA
CLK_SMBCLK



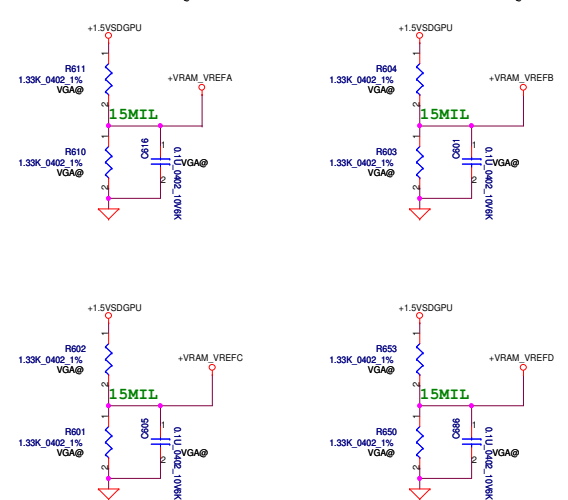
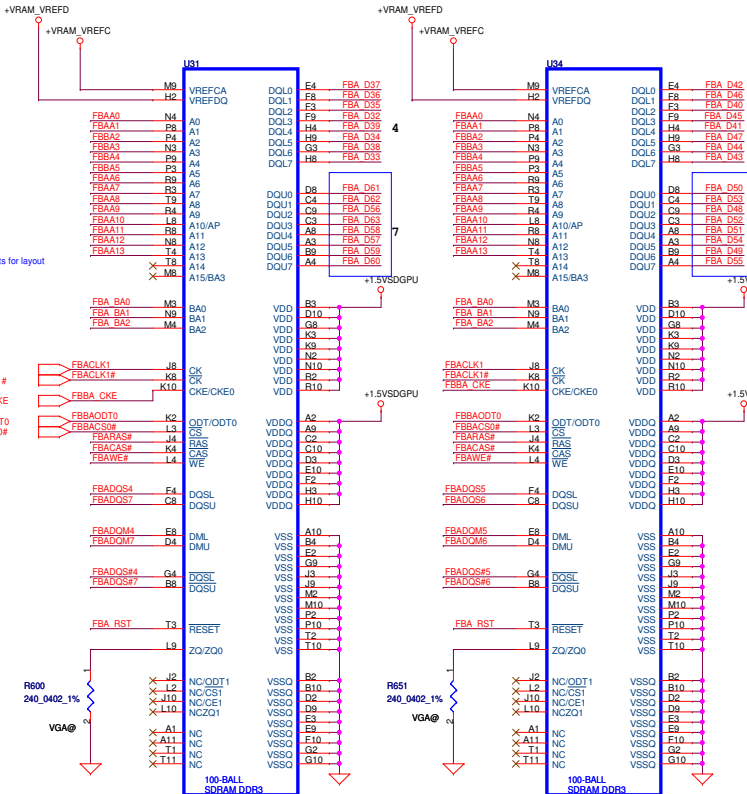
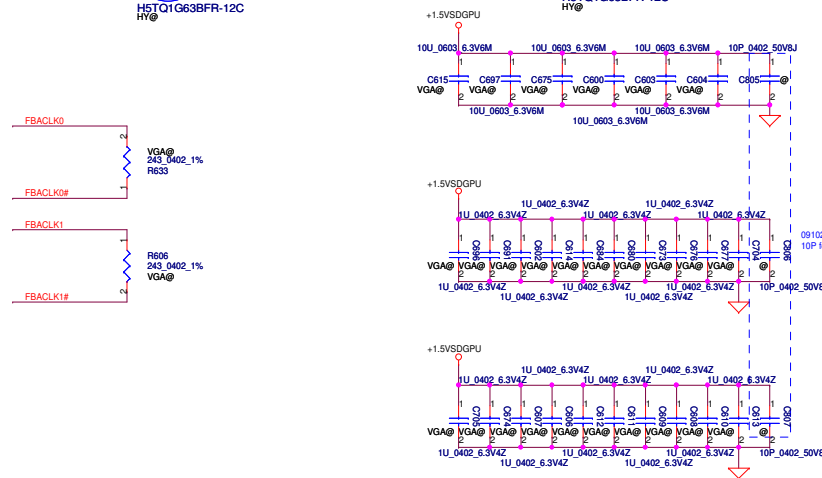
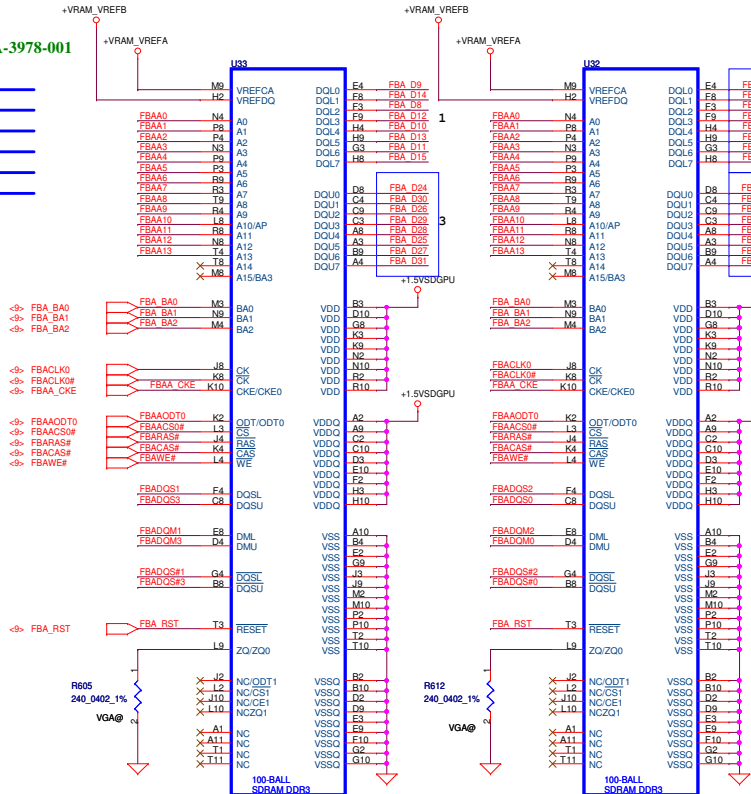
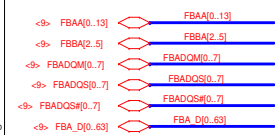
DIMMA

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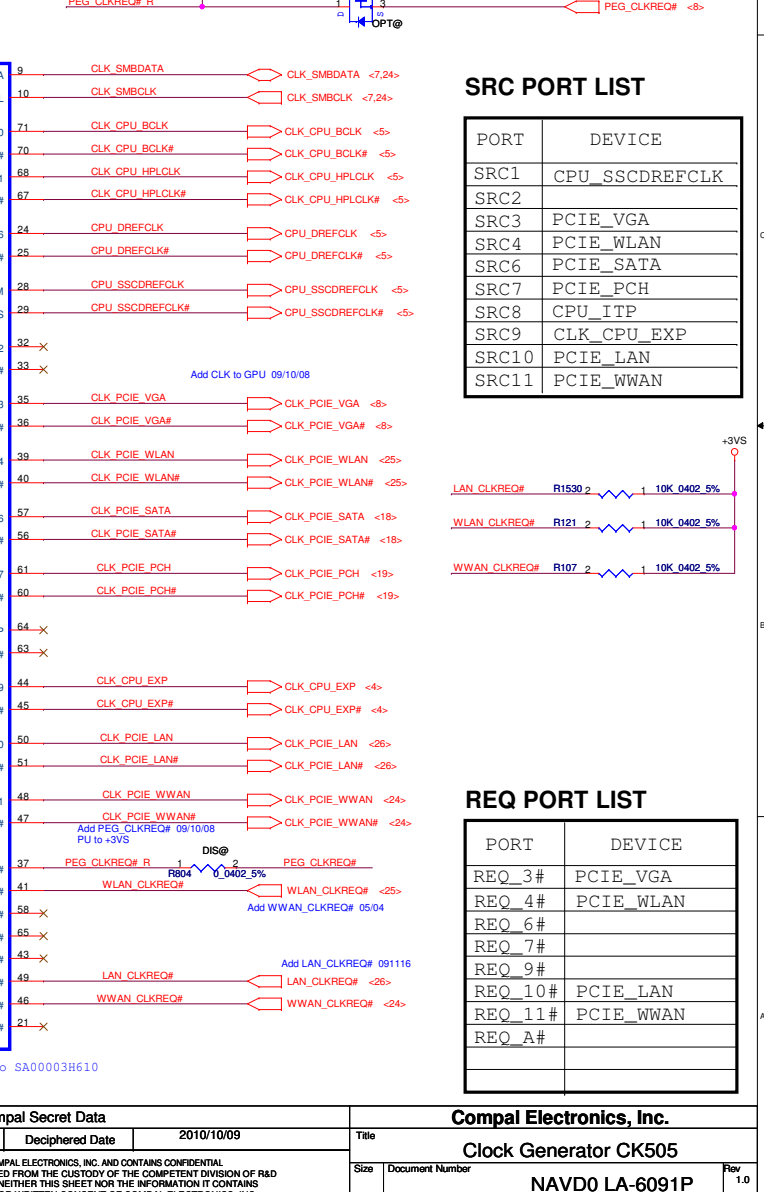
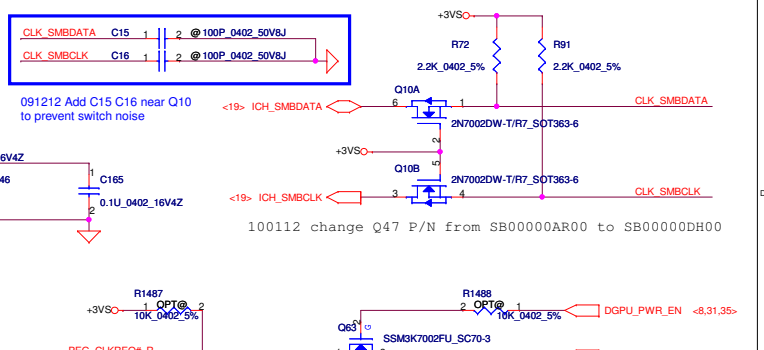
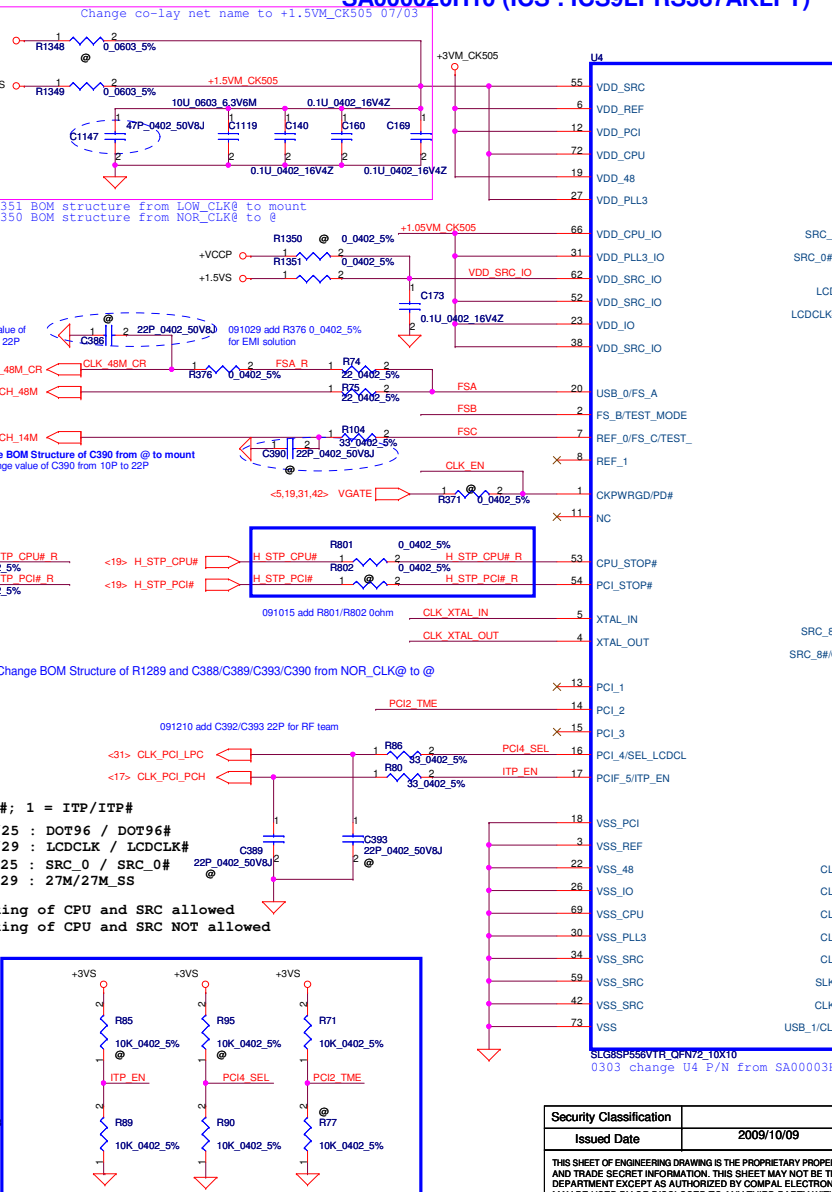
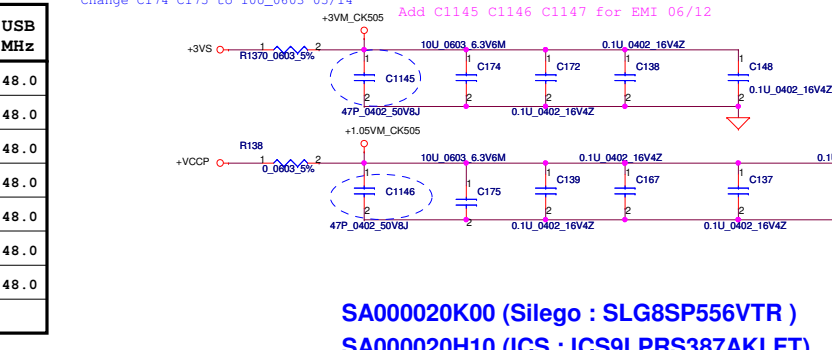
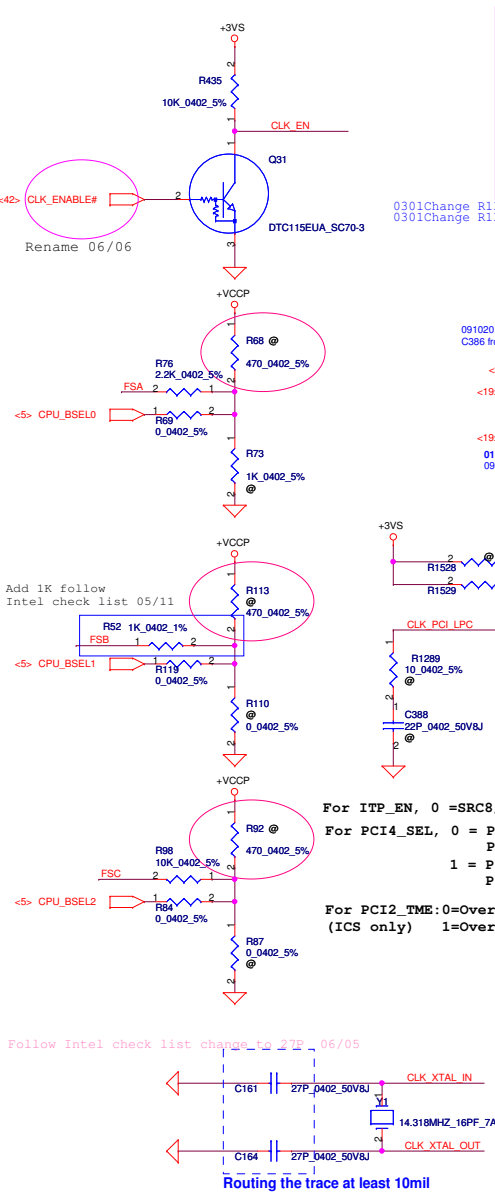


N10x 40nm DDR3 MAPPING
NVIDIA DOCUMENT FOR DA-3978-001



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FSC	FSB	FSA	CPU	SRC	PCI	REF	DOT_96	USB
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz	MHz	MHz	MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1						
Reserved								



SRC PORT LIST

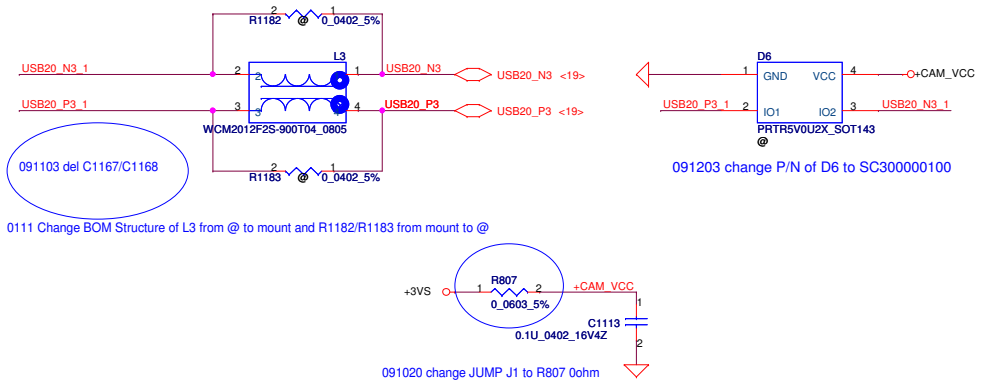
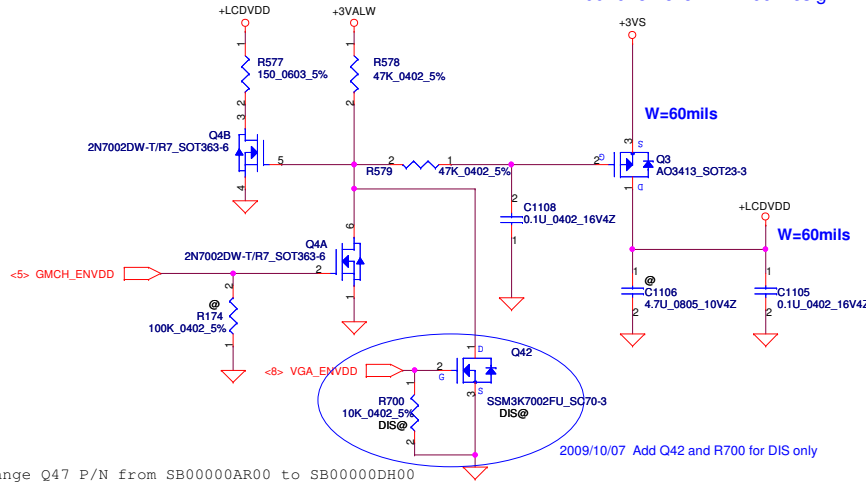
PORT	DEVICE
SRC1	CPU_SSCDREFCLK
SRC2	
SRC3	PCIE_VGA
SRC4	PCIE_WLAN
SRC6	PCIE_SATA
SRC7	PCIE_PCH
SRC8	CPU_ITP
SRC9	CLK_CPU_EXP
SRC10	PCIE_LAN
SRC11	PCIE_WWAN

REQ PORT LIST

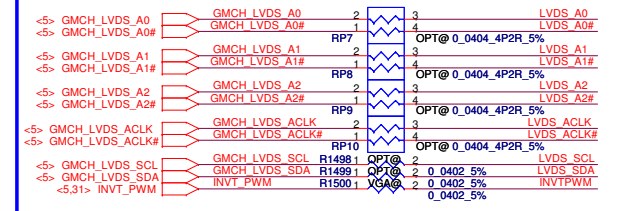
PORT	DEVICE
REQ_3#	PCIE_VGA
REQ_4#	PCIE_WLAN
REQ_6#	
REQ_7#	
REQ_9#	
REQ_10#	PCIE_LAN
REQ_11#	PCIE_WWAN
REQ_A#	

LCD POWER CIRCUIT

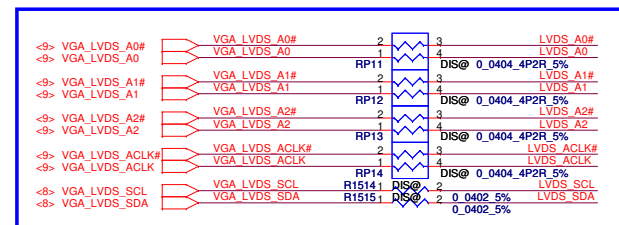
091015 follow NTV00 Design



OPTIMUS



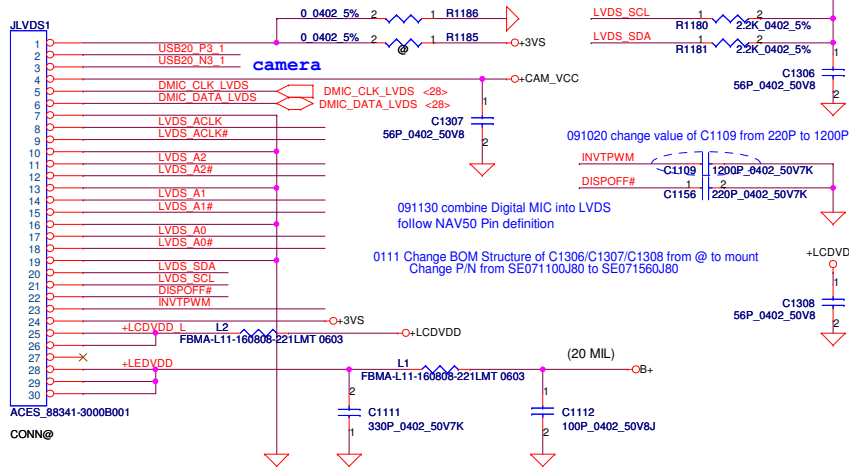
DIS ONLY



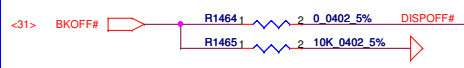
CMOS & LCD/PANEL BD. Conn.

Modify JLVDS1 08/04

20100106 add R1186 connect pin1 of JLVDS1 to GND



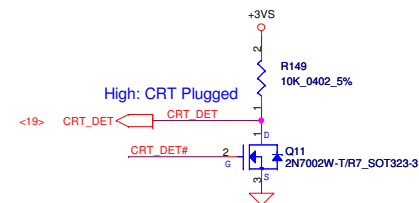
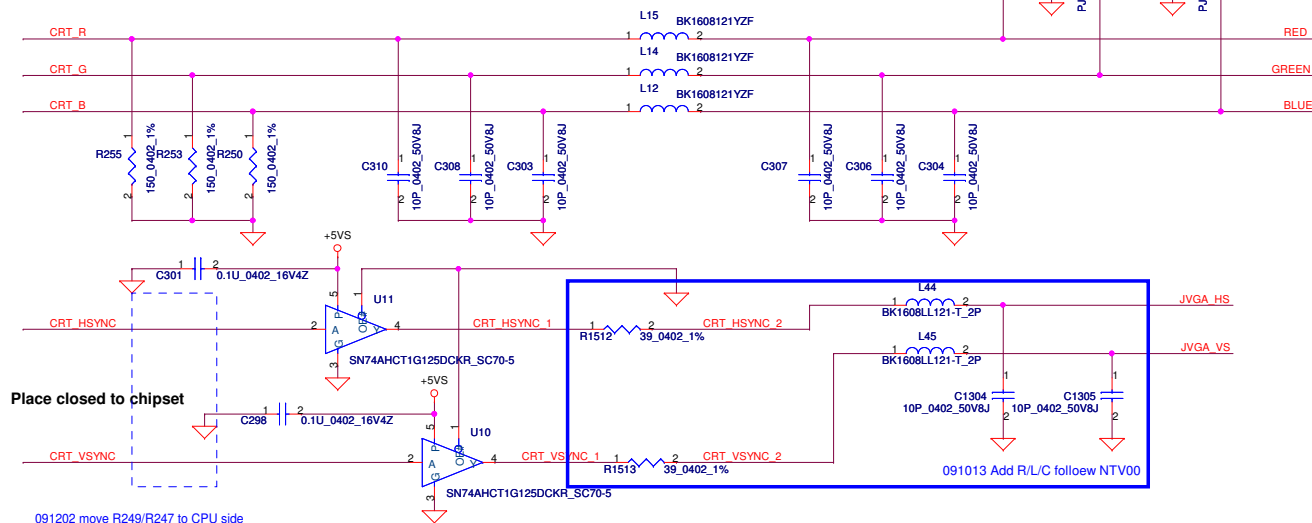
LED PANEL Conn.



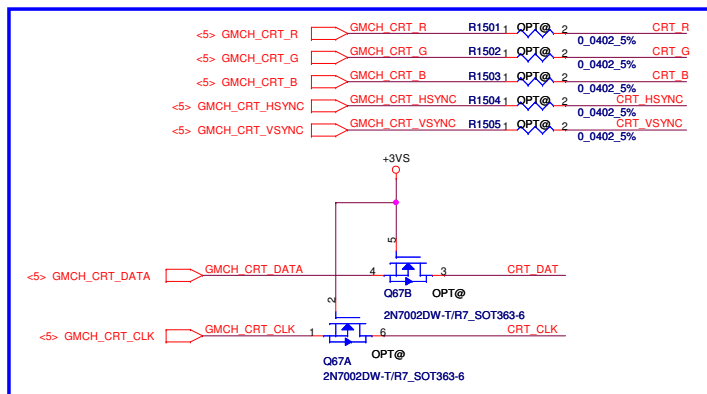
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CRT PORT

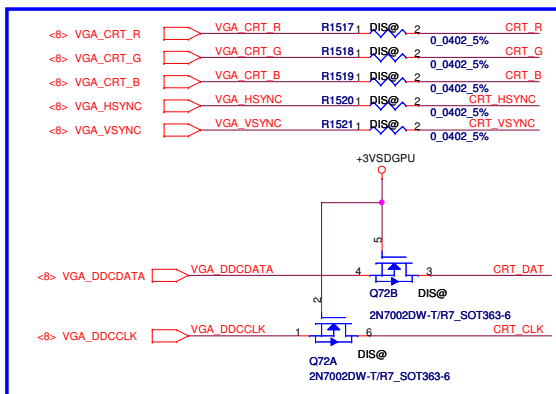
Modify C31- C308 C303 C307 C306 C304 BOM Structure 0615
0120 Change L12,L14,L15 P/N from SM01000AL00 to SM010032020



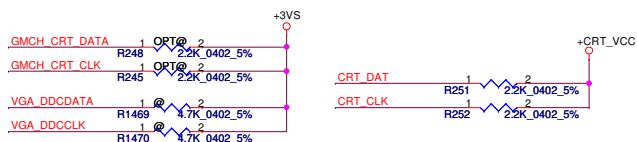
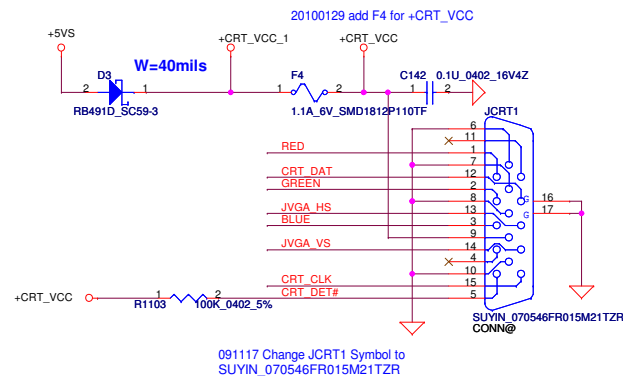
OPTIMUS



DIS ONLY

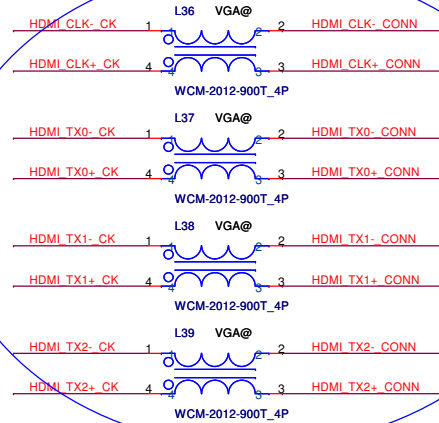


100112 change Q72 P/N from SB00000AR00 to SB00000DH00

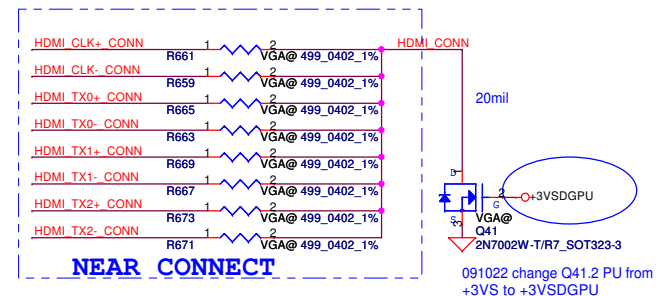


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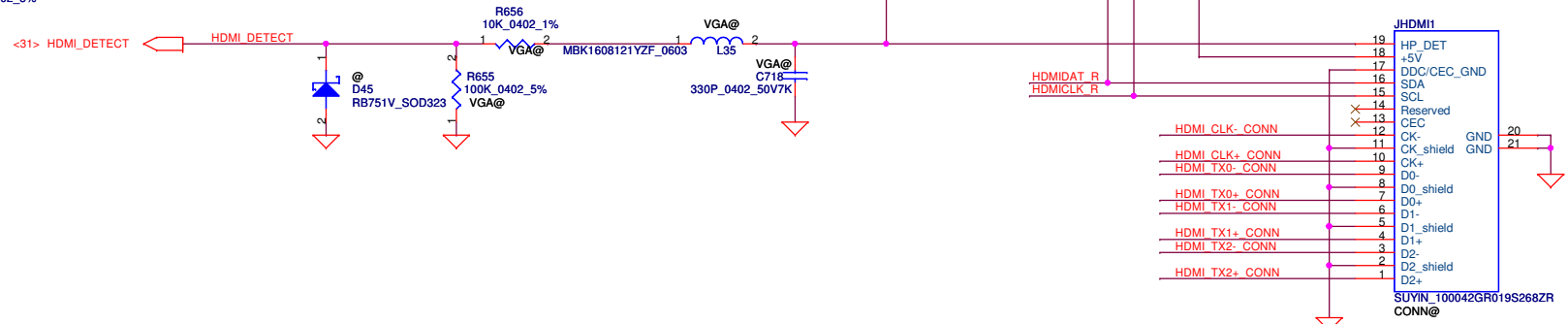
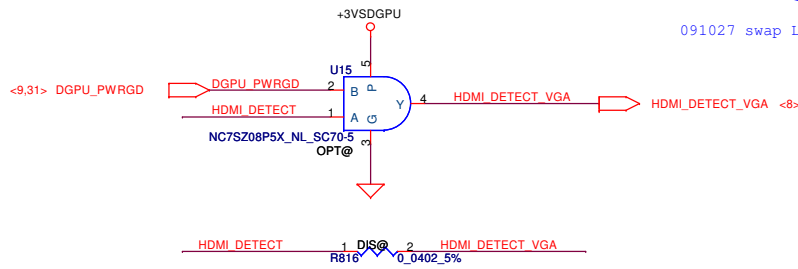
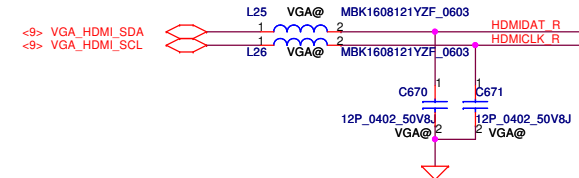
<9> VGA_HDMI_CLK+	C669	1	2	VGA@ 0.1U_0402_16V7K	HDMI_CLK+_CK	R660	1	2	0.0402_5%	HDMI_CLK+_CONN
<9> VGA_HDMI_CLK-	C668	1	2	VGA@ 0.1U_0402_16V7K	HDMI_CLK-_CK	R658	1	2	0.0402_5%	HDMI_CLK-_CONN
<9> VGA_HDMI_TX0+	C667	1	2	VGA@ 0.1U_0402_16V7K	HDMI_TX0+_CK	R664	1	2	0.0402_5%	HDMI_TX0+_CONN
<9> VGA_HDMI_TX0-	C666	1	2	VGA@ 0.1U_0402_16V7K	HDMI_TX0-_CK	R662	1	2	0.0402_5%	HDMI_TX0-_CONN
<9> VGA_HDMI_TX1+	C715	1	2	VGA@ 0.1U_0402_16V7K	HDMI_TX1+_CK	R668	1	2	0.0402_5%	HDMI_TX1+_CONN
<9> VGA_HDMI_TX1-	C713	1	2	VGA@ 0.1U_0402_16V7K	HDMI_TX1-_CK	R666	1	2	0.0402_5%	HDMI_TX1-_CONN
<9> VGA_HDMI_TX2+	C730	1	2	VGA@ 0.1U_0402_16V7K	HDMI_TX2+_CK	R672	1	2	0.0402_5%	HDMI_TX2+_CONN
<9> VGA_HDMI_TX2-	C711	1	2	VGA@ 0.1U_0402_16V7K	HDMI_TX2-_CK	R670	1	2	0.0402_5%	HDMI_TX2-_CONN



091027 swap L36/L37/L38/L39 nets for layout

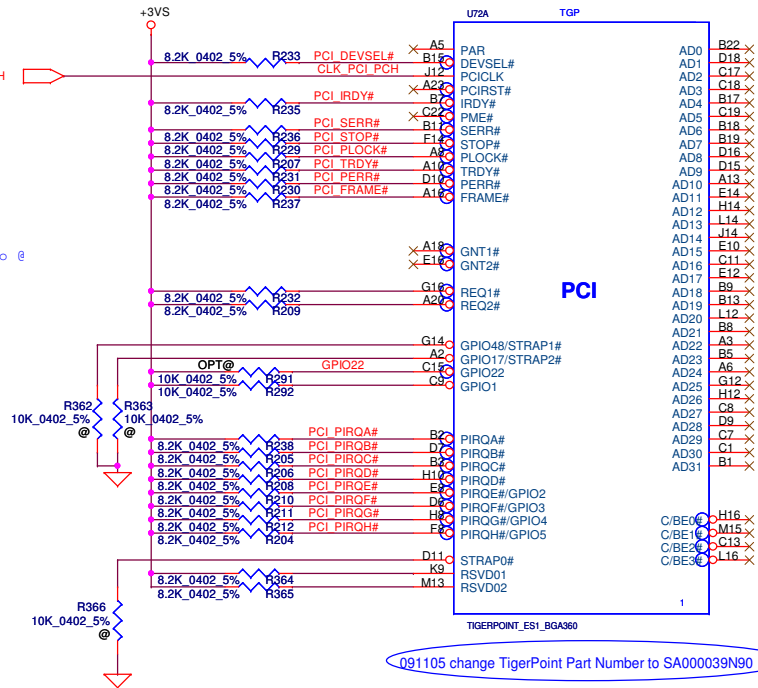
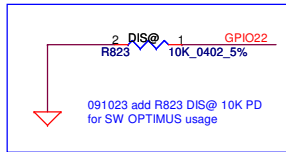
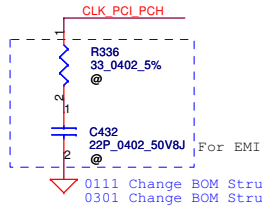


091022 change Q41.2 PU from +3VS to +3VSDGPU



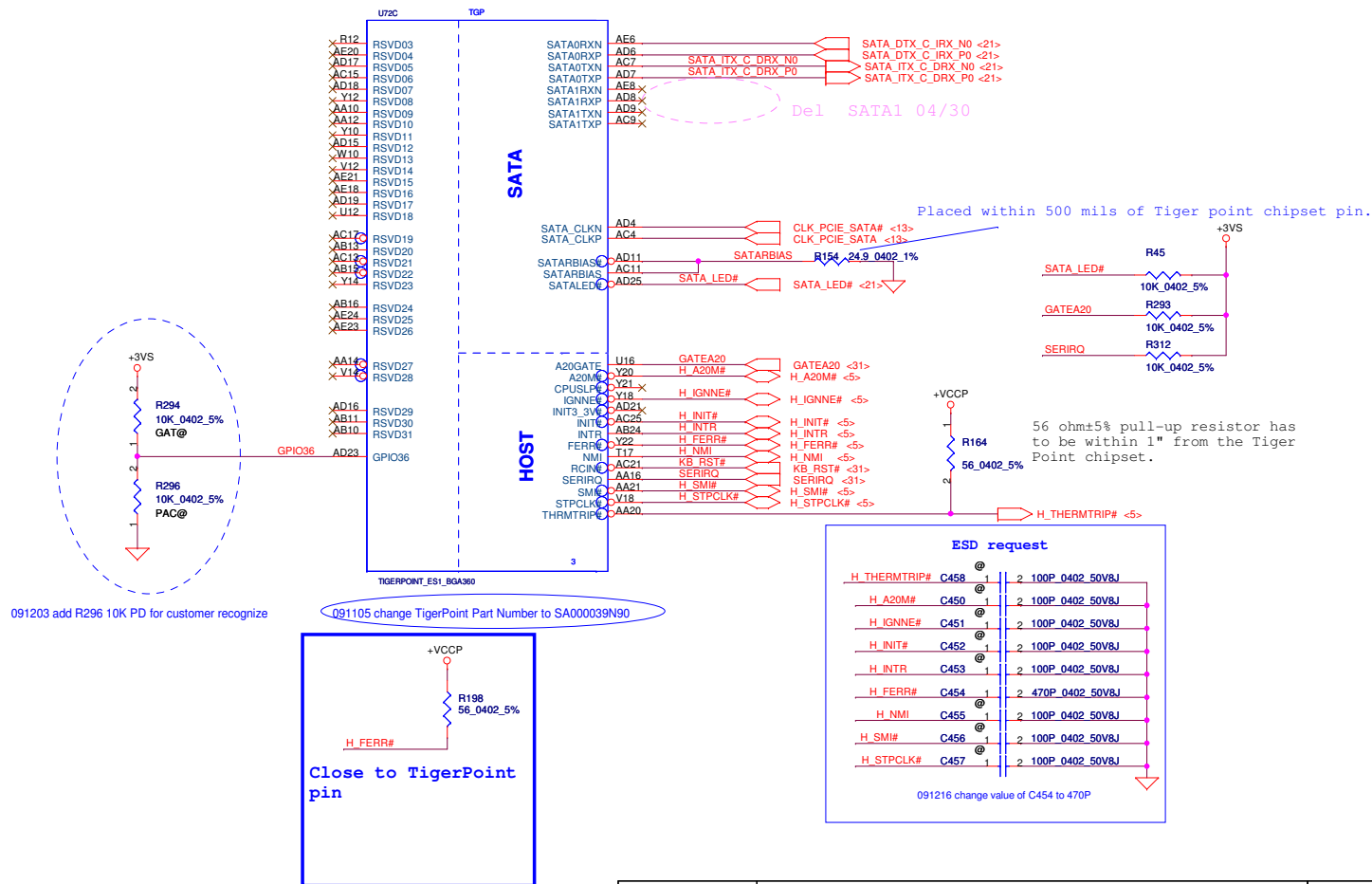
091012 change HDMI CONN Symbol to SUYIN_100042GR019S268ZR

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STRAP2# GPIO17	STRAP1# GPIO48	Boot BIOS
0	1	SPI
1	0	PCI
1	1	LPC

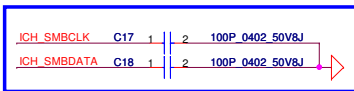
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Issued Date	2009/10/09	Deciphered Date	2010/10/09	Title	
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				Tigerpoint(2/4)	
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				Custom	NAVD0 LA-6091P
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091212 Add C30 near PCH to prevent switch noise

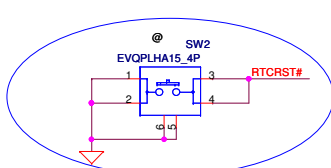
HDA_SDI0_C30 1 2 @100P_0402_50V8J



091212 Add C17 C18 near U72 to prevent switch noise

091105 change TigerPoint Part Number to SA000039N90

20100120 change SW2 from mount to @



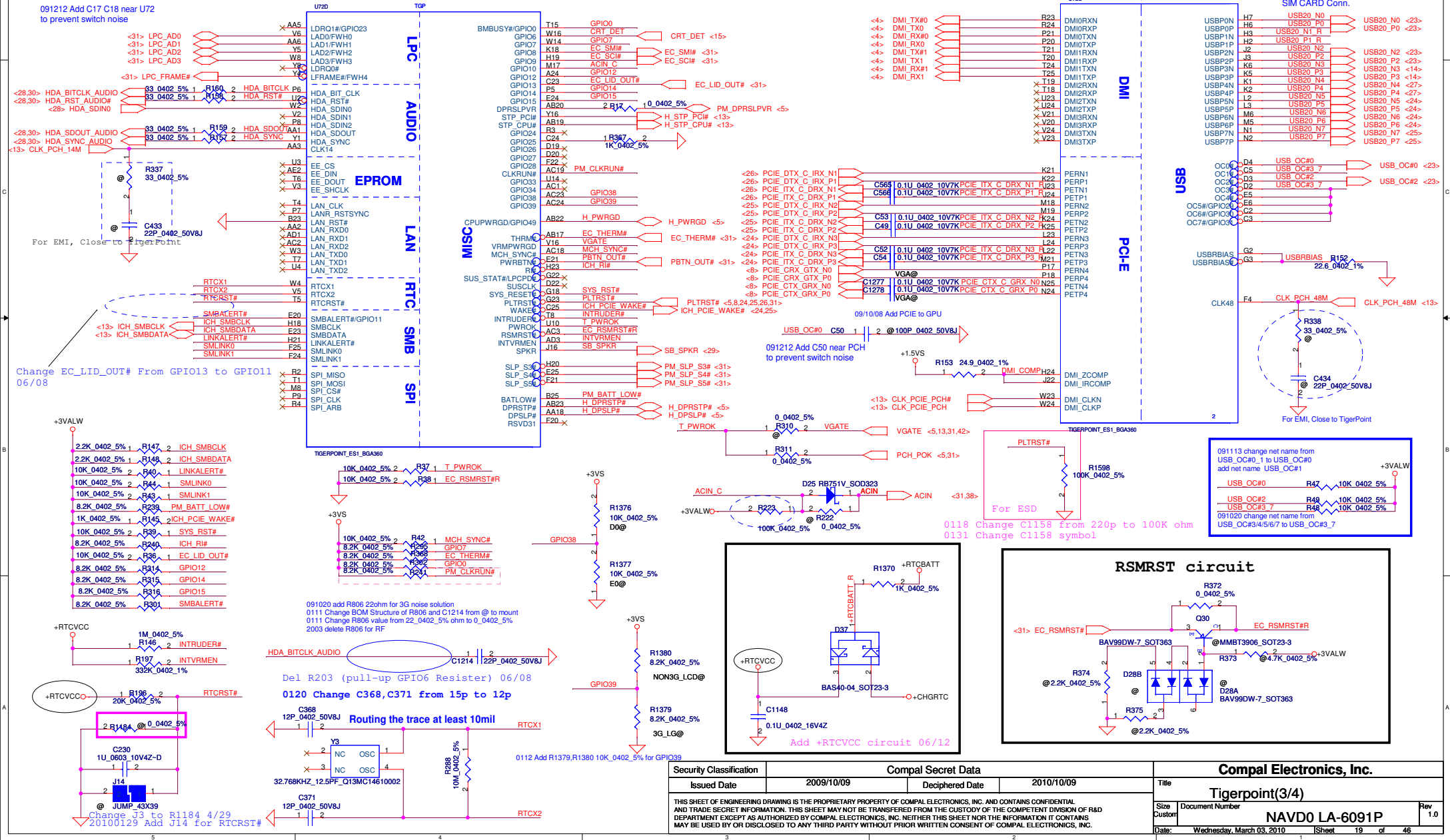
PCIE Port List	
1	LAN
2	WLAN
3	WWAN
4	



091105 change TigerPoint Part Number to SA000039N90

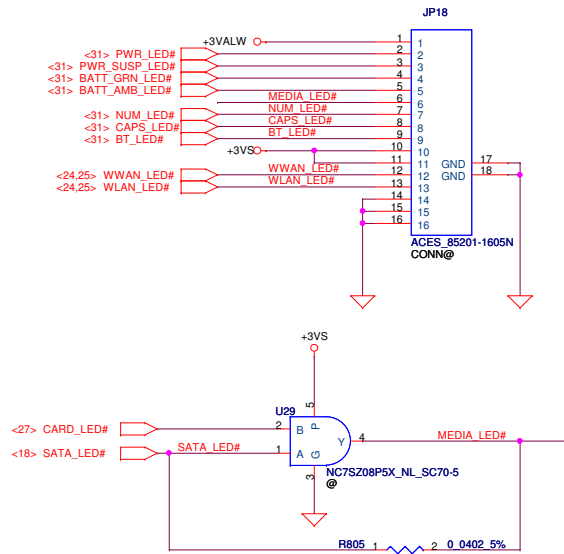
USB Port List	
0	USB Left1
1	
2	USB Right2
3	CMOS
4	CardReader
5	WWAN
6	BT
7	WIMAX

091204 add USB20_N1/P1 for SIM CARD Conn.

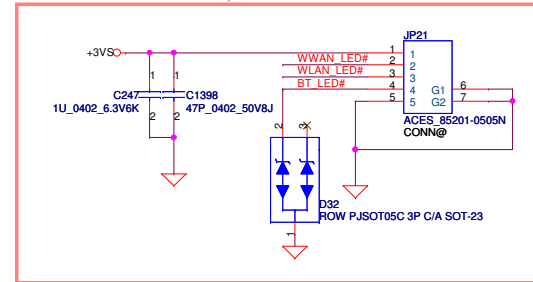


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Title			
Tigerpoint(3/4)			
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LED PCB CONN

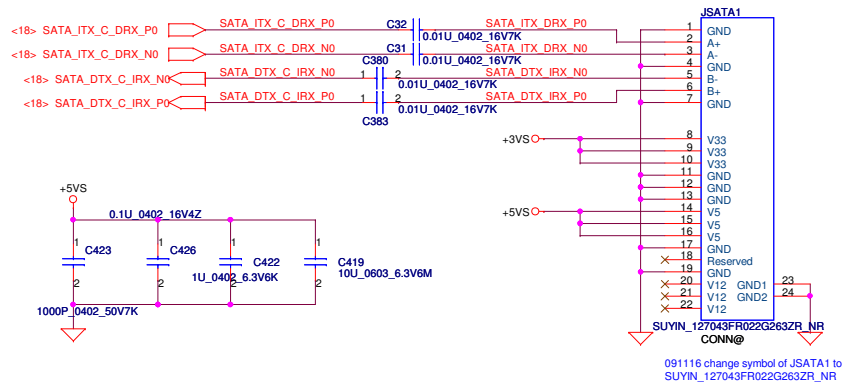


09/30 add ESD



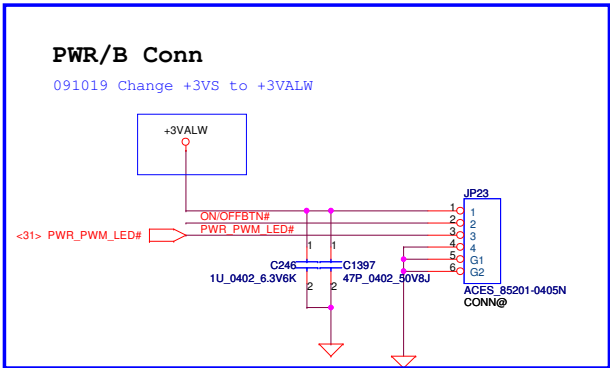
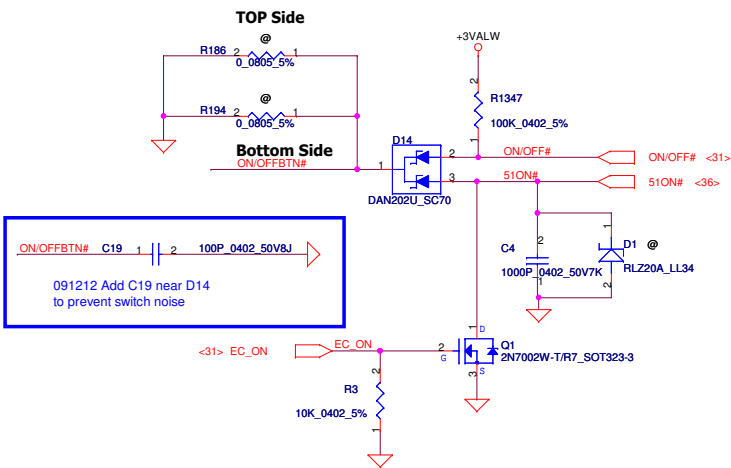
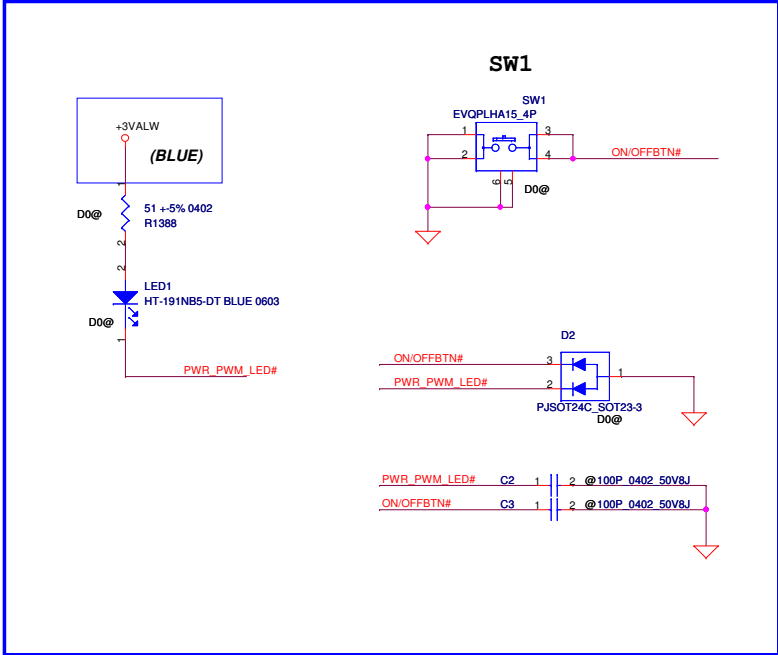
0108 Add C247,C1398 on pin1 of JP21 (RF)

SATA HDD Conn.

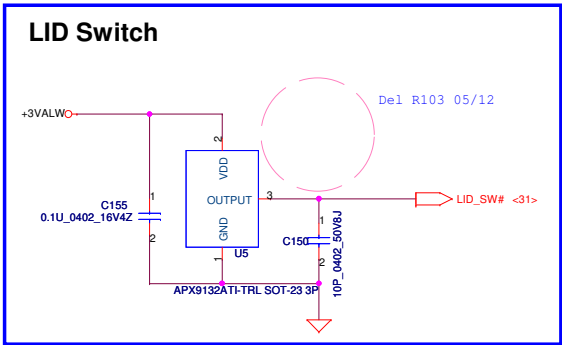


091116 change symbol of JSATA1 to
SUYIN_127043FR022G263ZR_NR

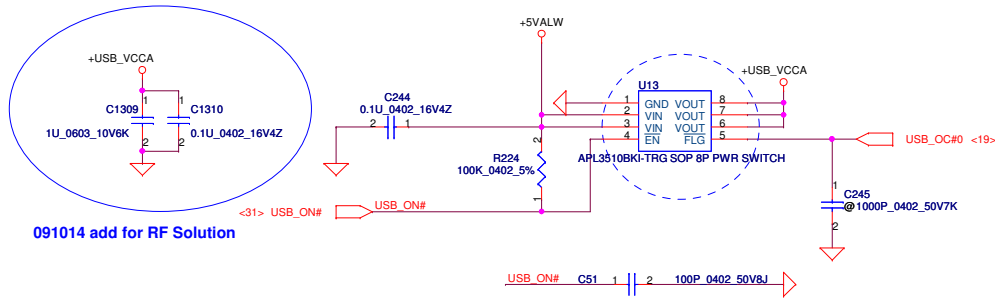
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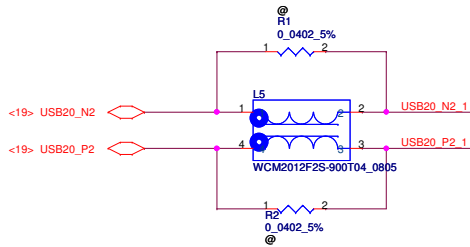
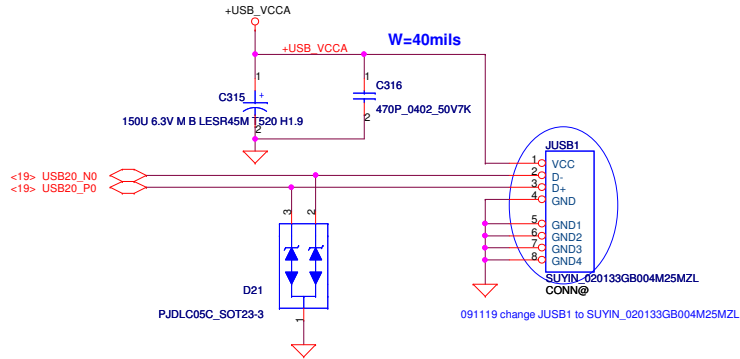
0108 Add C246,C1397 on pin1 of JP23



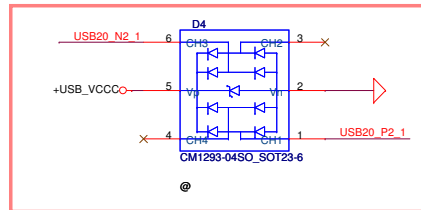
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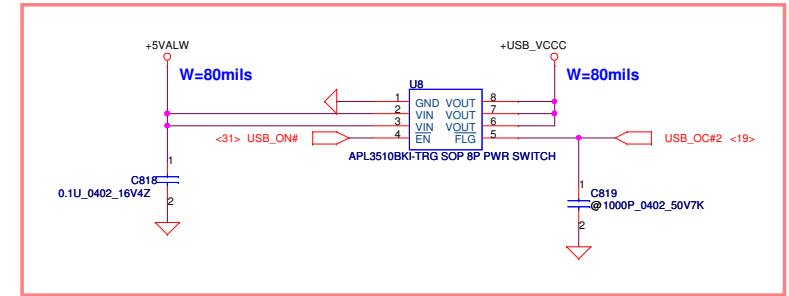
USB CONN.1



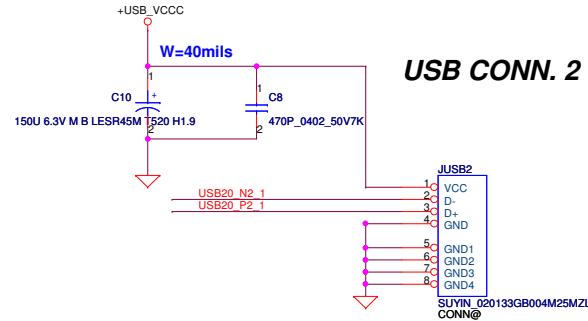
5/12 Revised net name



5/5 Add U2 circuit



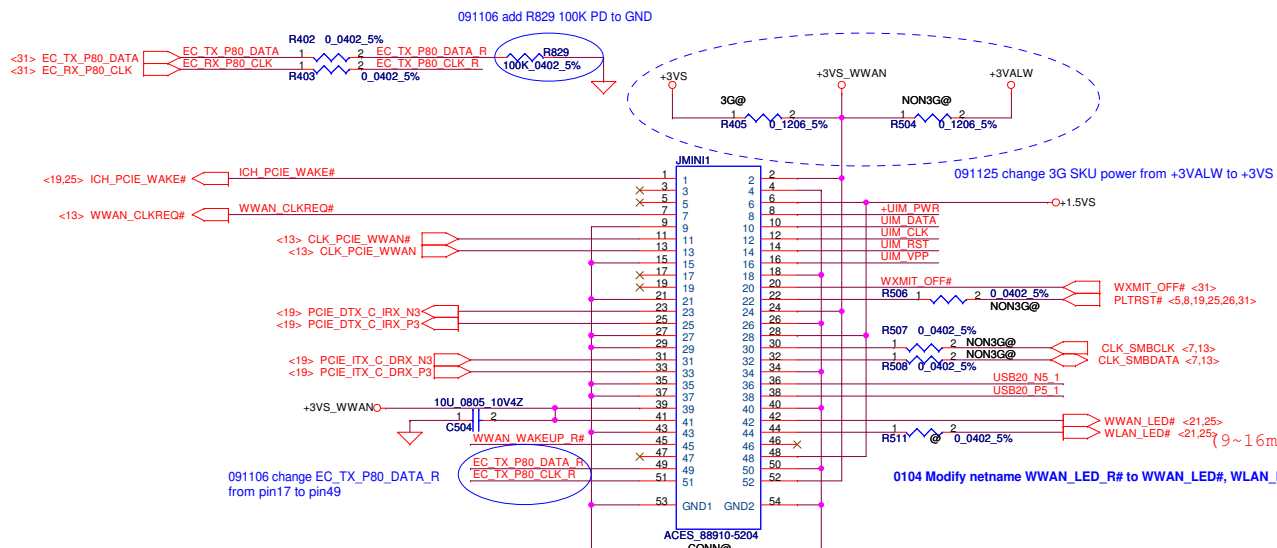
USB CONN. 2



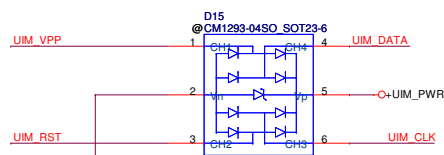
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2009/10/09				2010/10/09				USB PORT			
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Mini-Express Card for WWAN

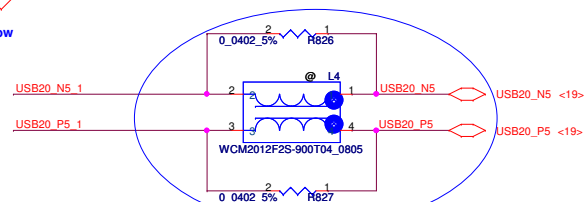
091019 Remove C1163/C1164/C1165/C1166



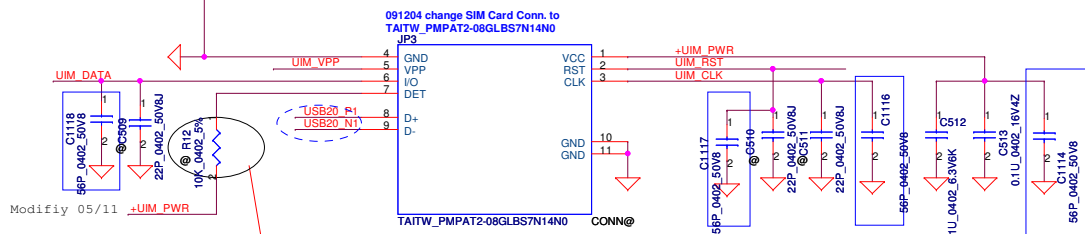
091012 Change Mini PCIE CONN
Symbol to ACES 88910-5204 follow
ME CONN LISTRev08



091204 change SIM Card Conn. to
TAITW_PMPAT2-08GLBS7N14N0
.IP3

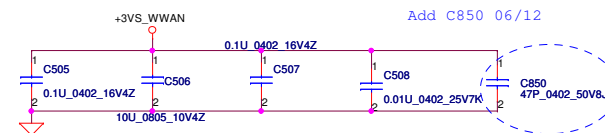


091102 add L4/R826/R827 on USB port5
follow RF team review



Reserve for SIM card does not meet rise time and pull-up is needed.

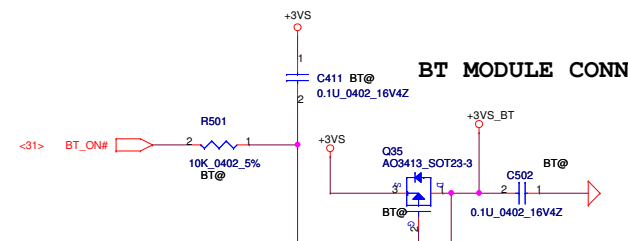
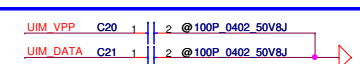
Add C1114 C1116 C1117 C1118 05/11
Change C512 to 1U 0402 05/14



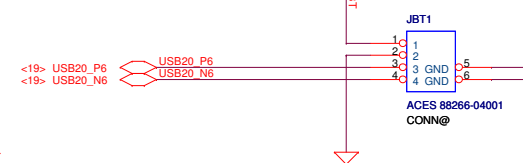
Add C850 06/12



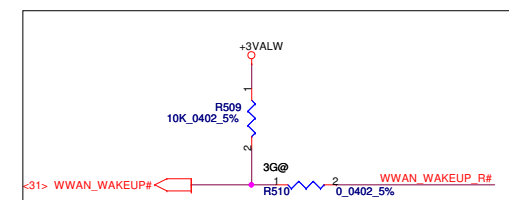
091212 Add C2
near JMINI1
to prevent switch



BT MODULE CONN



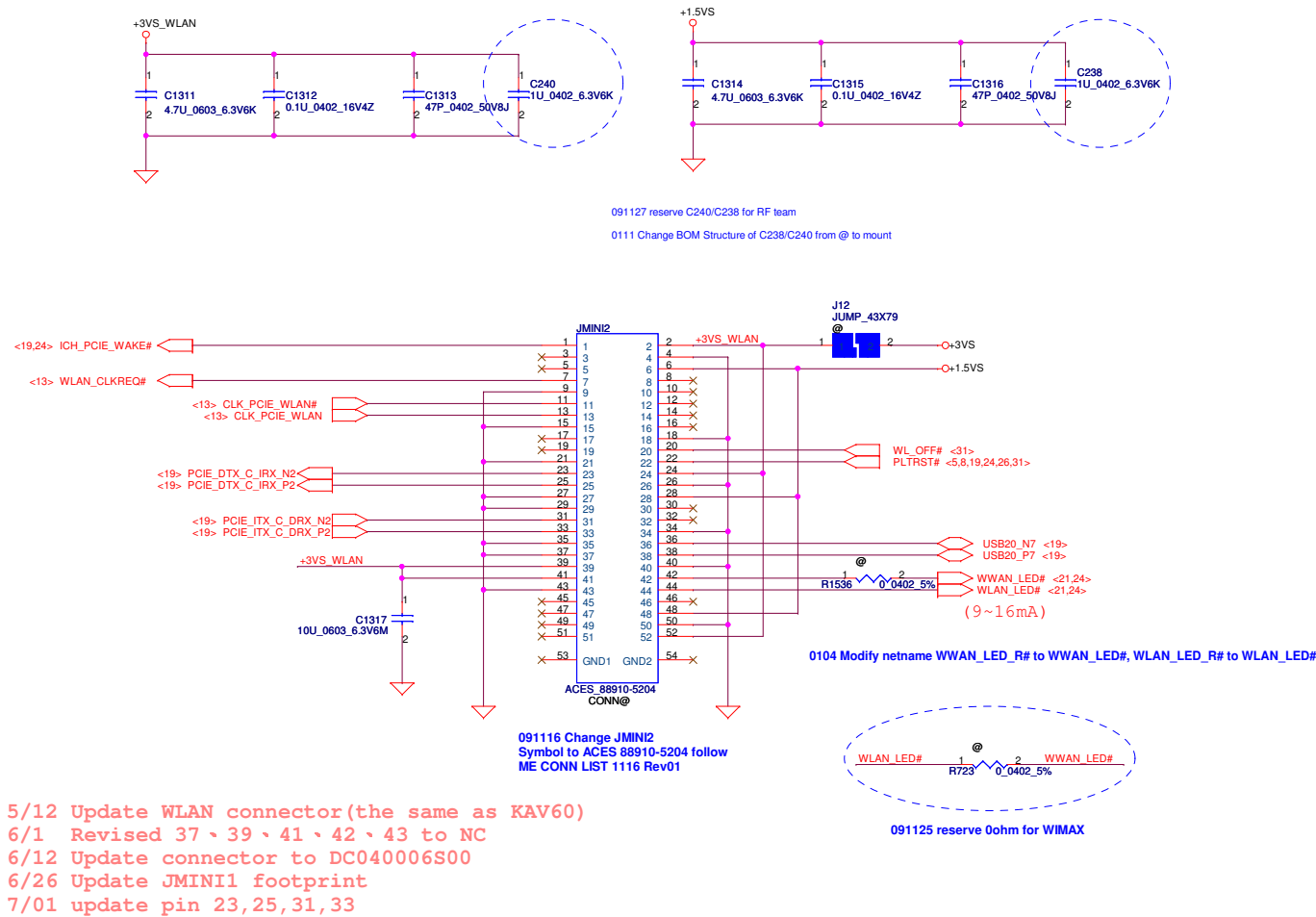
ACES 88266-04001
CONN@



<31>

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Mini-Express Card for WLAN



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				Size Custom	Document Number NAVD0 LA-6091P
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091020 change JUMP J2/J3 to R808/R809 0ohm

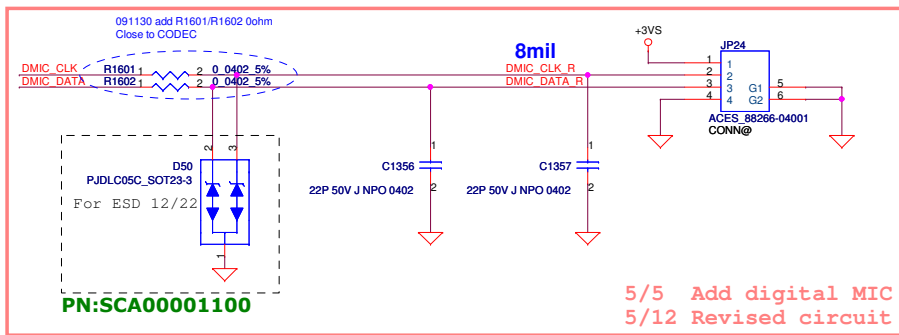
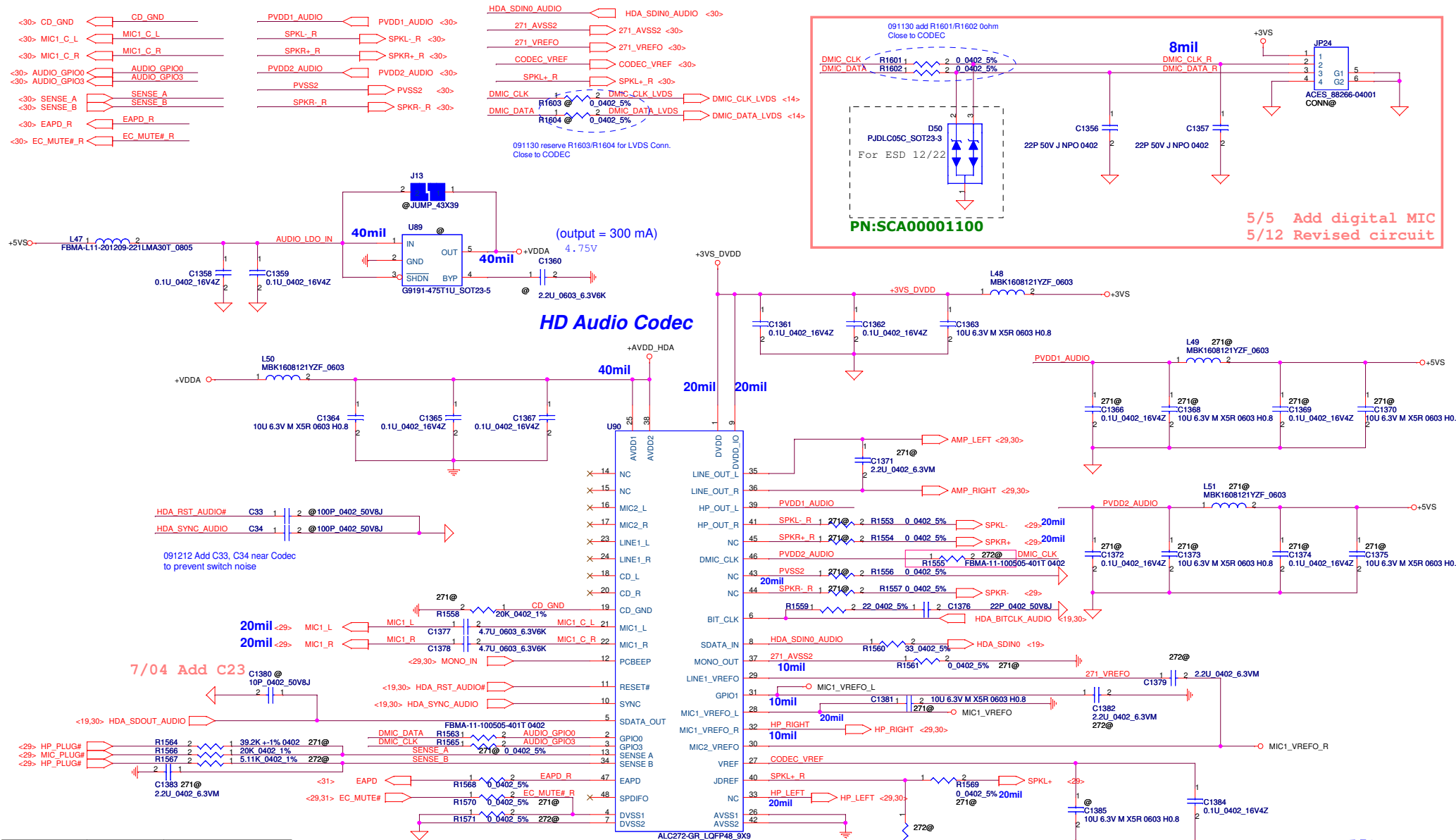
U1 close to JREAD1

If use external crystal(Y6),
U78 will change UB6252

Card Reader Connector

091203 change BOM structure of
Q53/R1395/R1396 from mount to @

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Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

Change to SA00002CI20 ALC272-VA2-GR



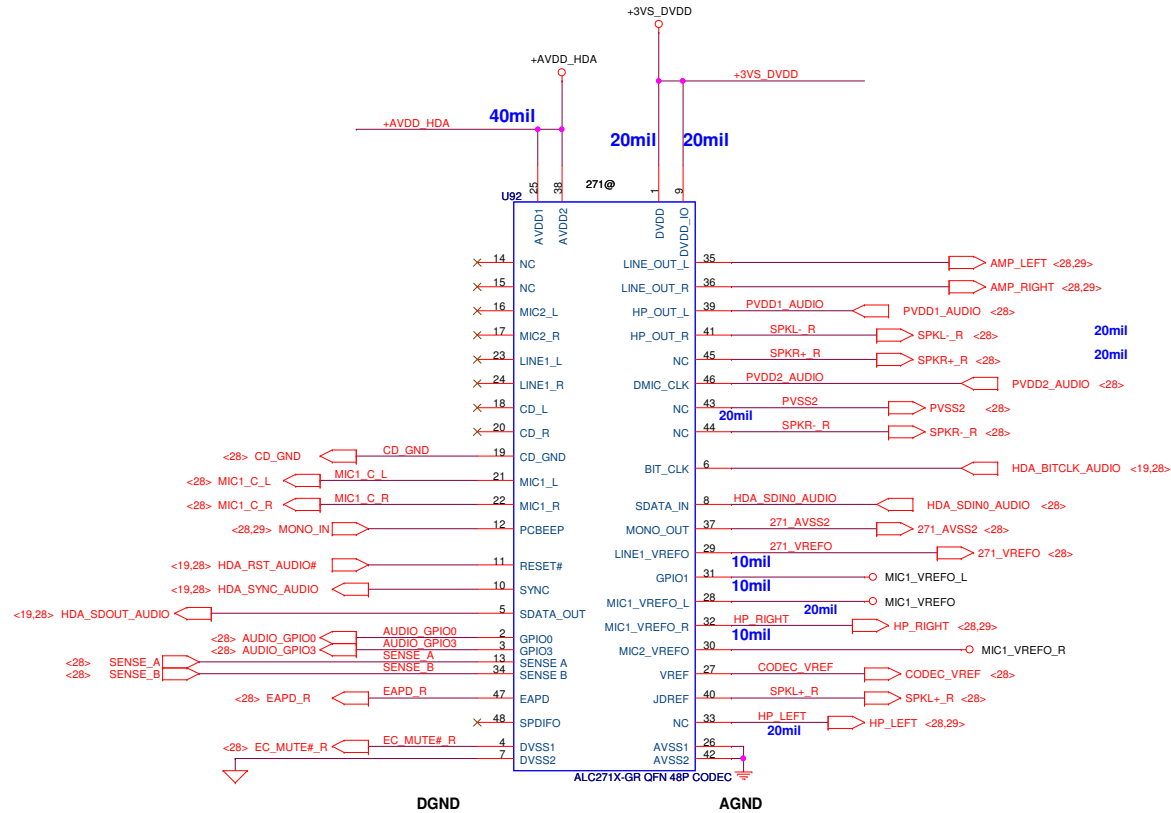
PCI Beep

091127 change value of R1328 from 10K to 4.7K



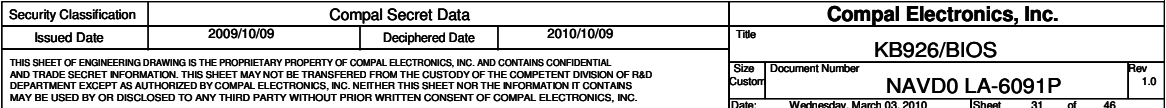
Security Classification		Compal Secret Data		Compal Electronics, Inc.				
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AMP & Audio Jack								
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						NAVD0 LA-6091P		
						Date:		Wednesday, March 03, 2010

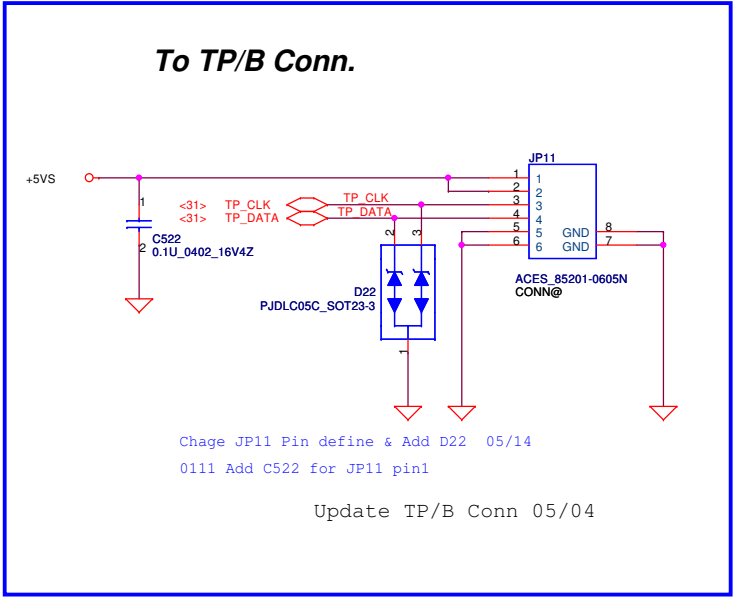
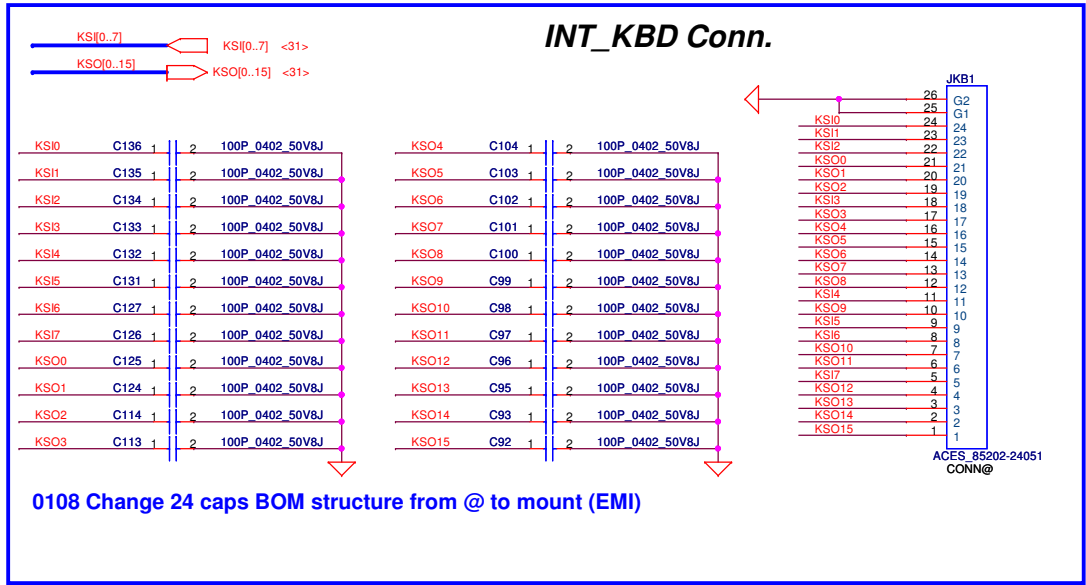
HD Audio Codec



Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

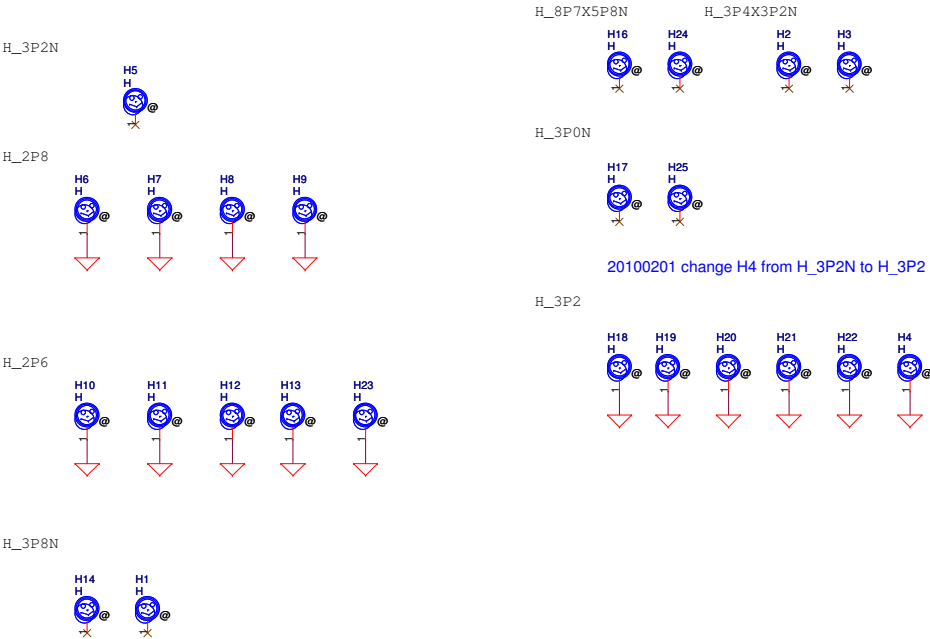
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Issued Date		2009/10/09		Deciphered Date		2010/10/09			
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				AUDIO CODEC ALC271					
				Size	Document Number			Rev	
				NAVD0 LA-6091P			1.0		
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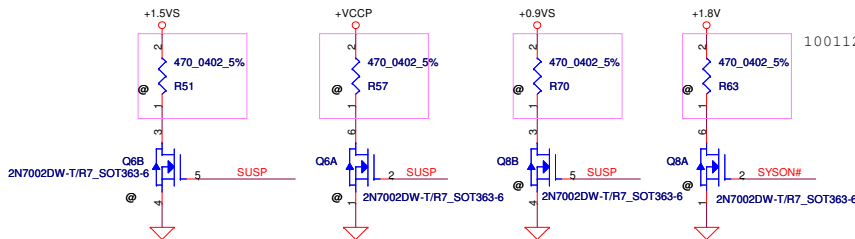
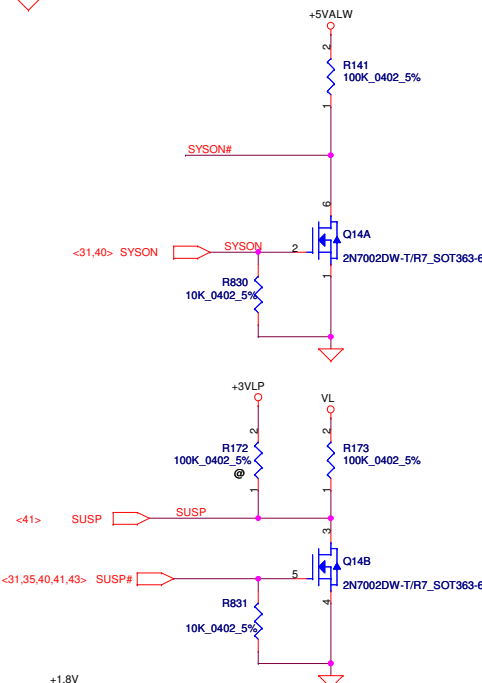
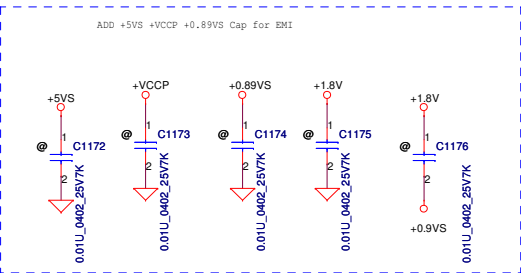
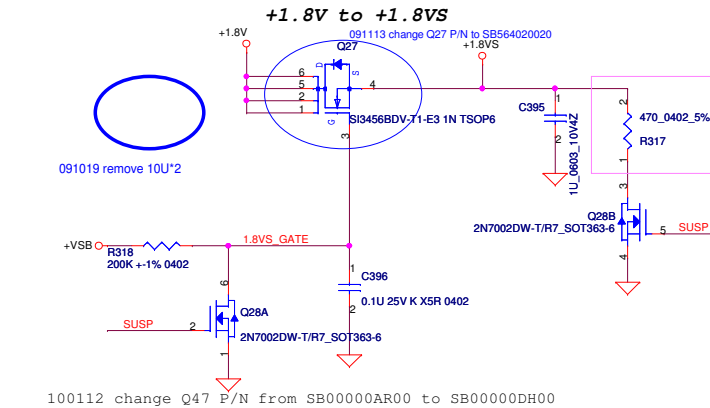
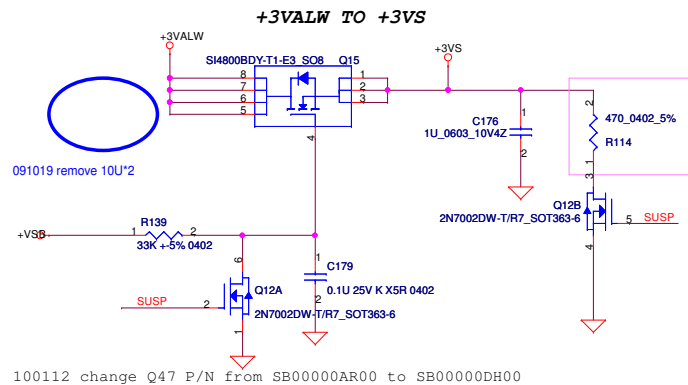
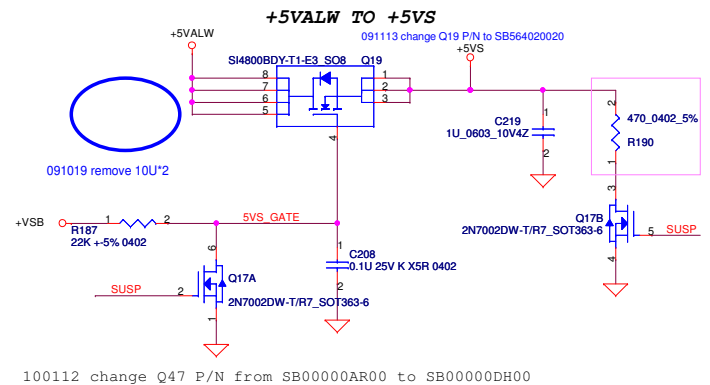


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				NAVD0 LA-6091P	
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				Sheet	32 of 46
				Rev	1.0

091028 Modify Hole location by 1127_NAVD0_NEW_MB_ASSY_FOR_2865_v11



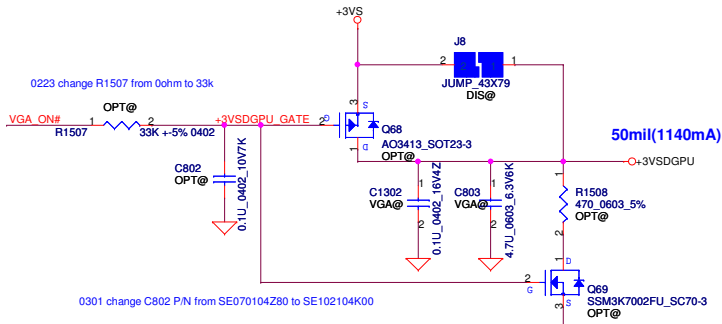
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				B	NAVDO LA-6091P
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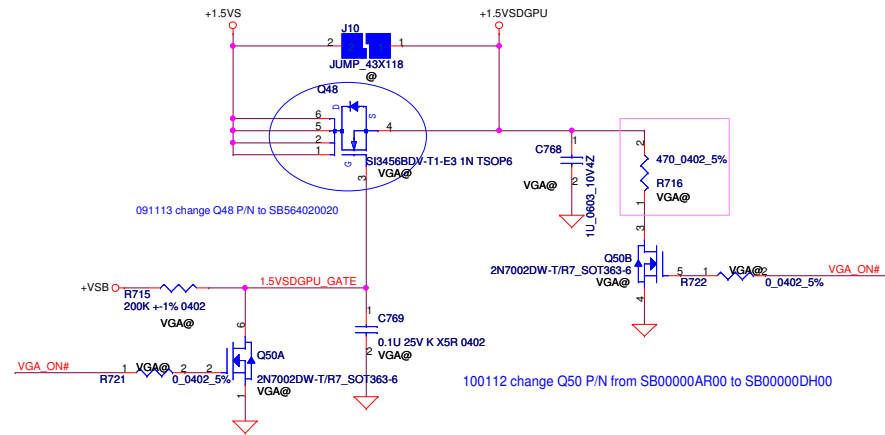
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						Size B		Document Number		NAVD0 LA-6091P		Rev 1.0	
						Date:		Wednesday, March 03, 2010		Sheet 34 of 46			

+3VS to +3VSDGPU Transfer

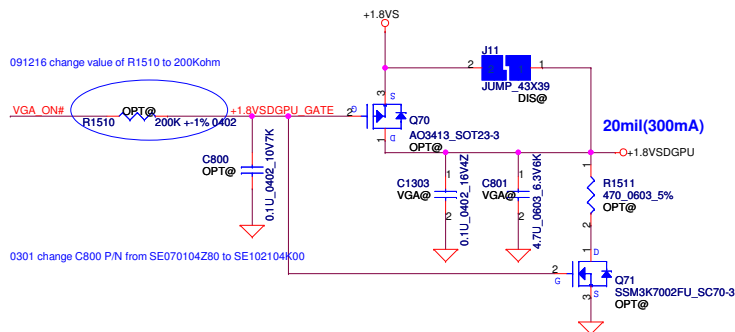
0111 Change BOM Structure of C1302/C803/C1303/C801/C1294 from OPT@ to VGA@



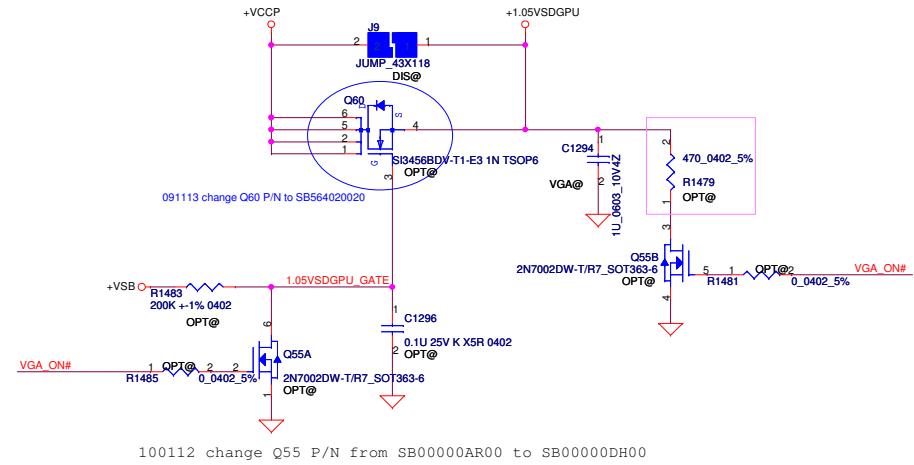
+1.5VS to +1.5VSDGPU Transfer



+1.8VS to +1.8VSDGPU Transfer



+VCCP to +1.05VSDGPU Transfer

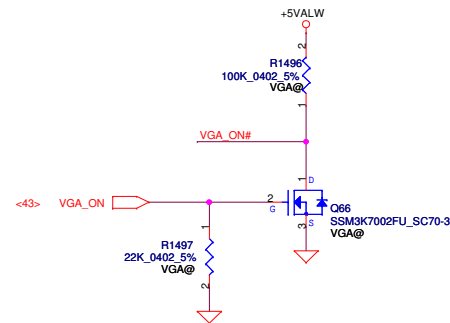


<8,13,31> DGPU_PWR_EN

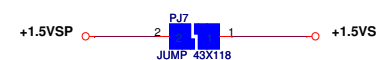
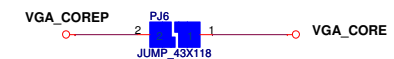
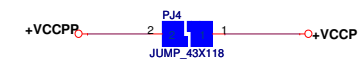
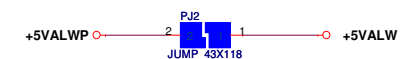
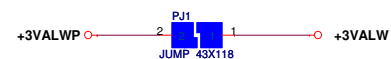
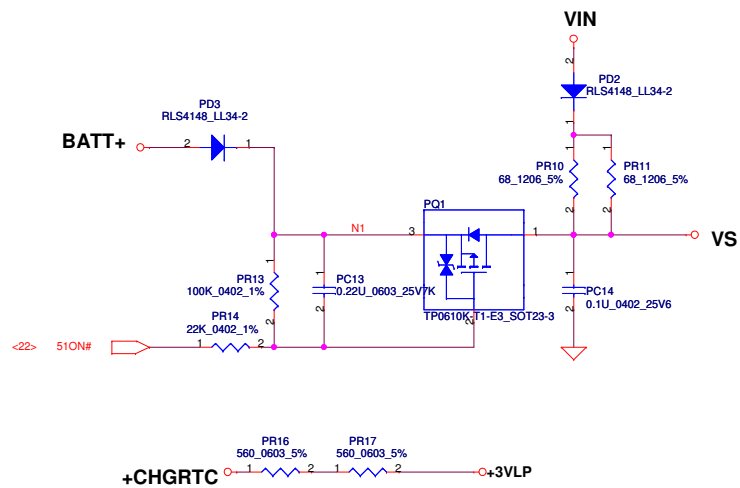
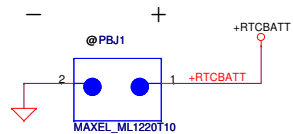
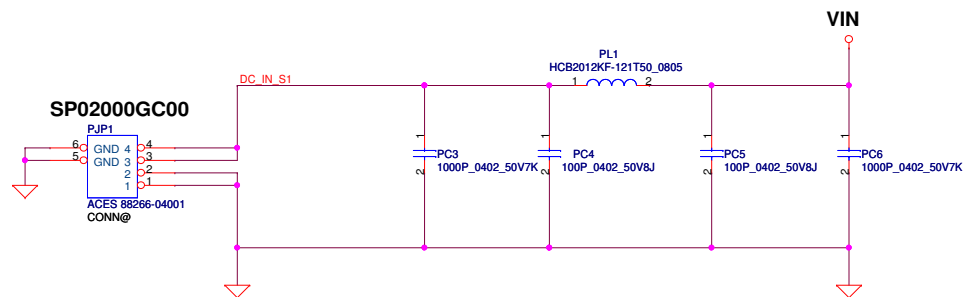
<31,34,40,41,43> SUSP#

VGA_ON C25 1 2 @100P 0402 50V8J

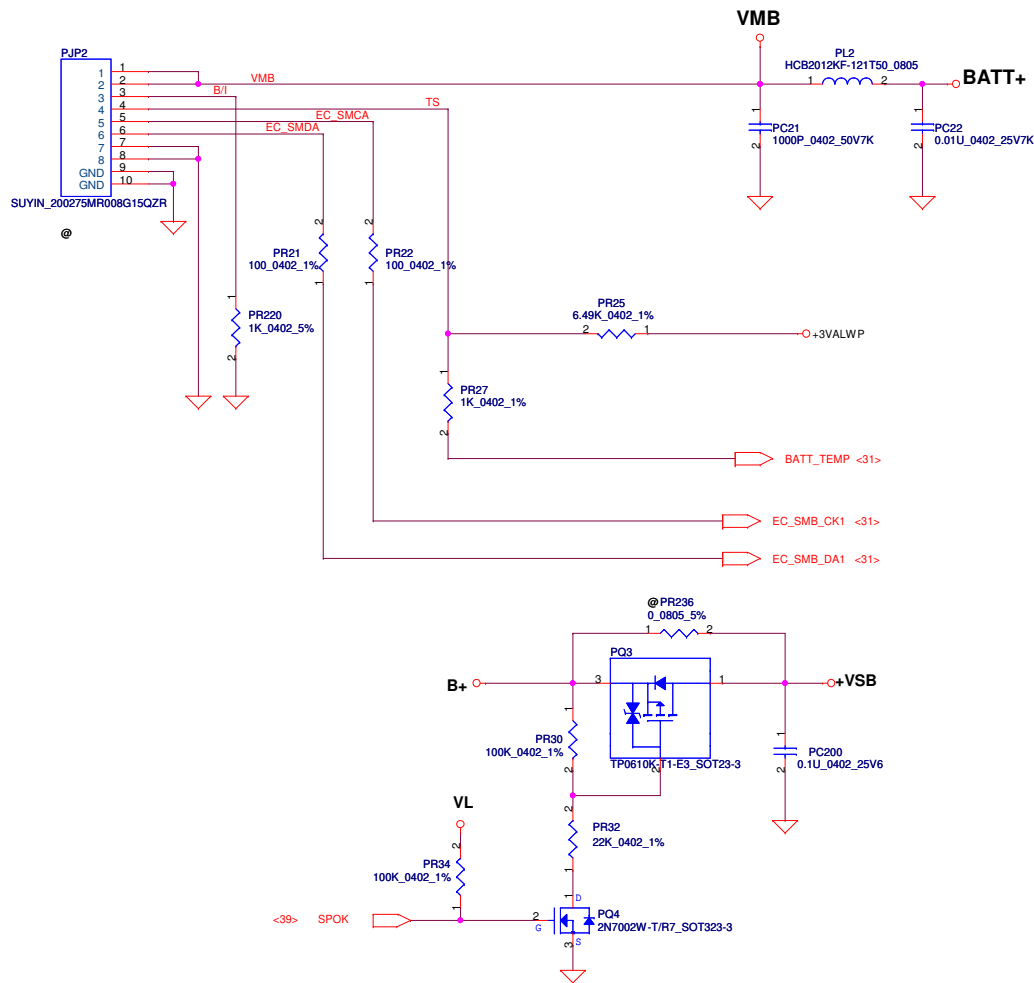
091212 Add C25 to prevent switch noise



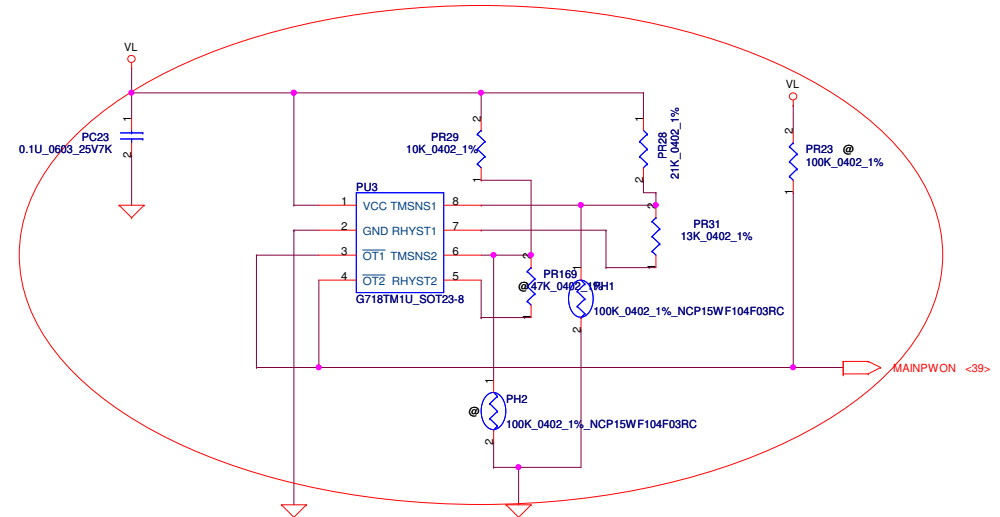
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				Size	Document Number	Rev
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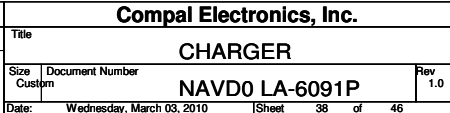
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Issued Date	2009/10/09	Deciphered Date	2010/10/09	Title	
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Size	Document Number	NAVD0 LA-6091P			Rev
Custom					1.0
Date:	Wednesday, March 03, 2010	Sheet	36	of	46

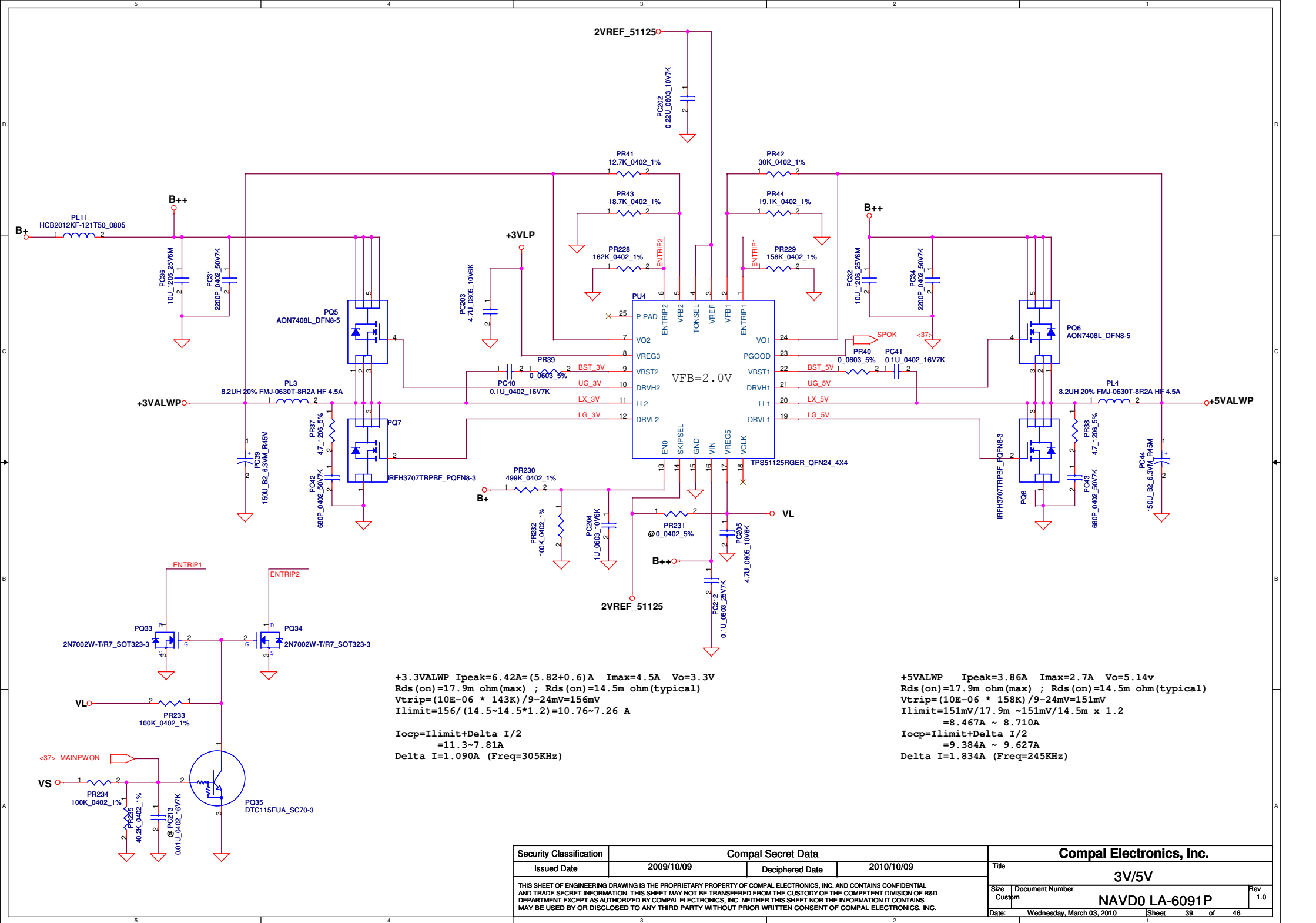


PH1 under CPU bottom side :
 CPU thermal protection at 92 degree C
 Recovery at 70 degree C

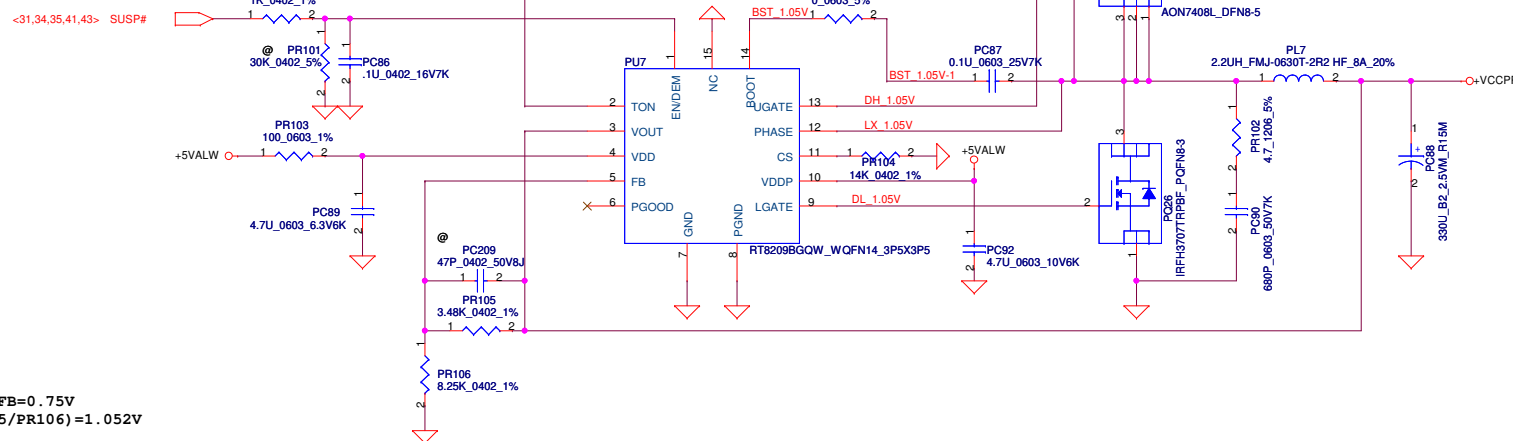
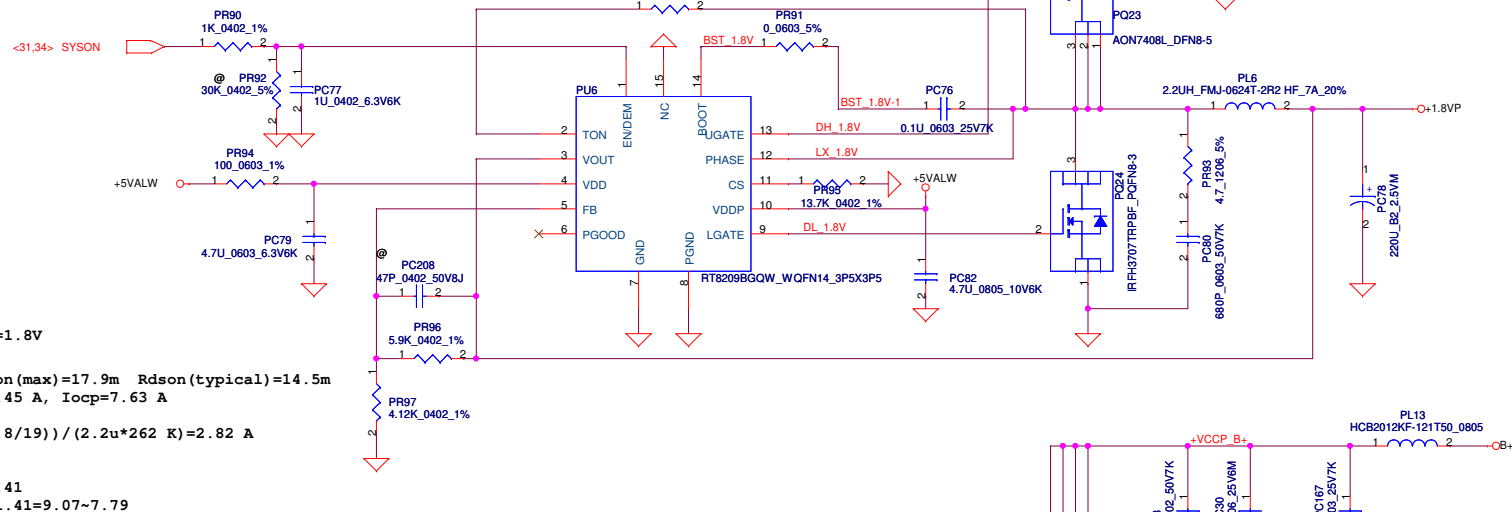


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				Rev	1.0





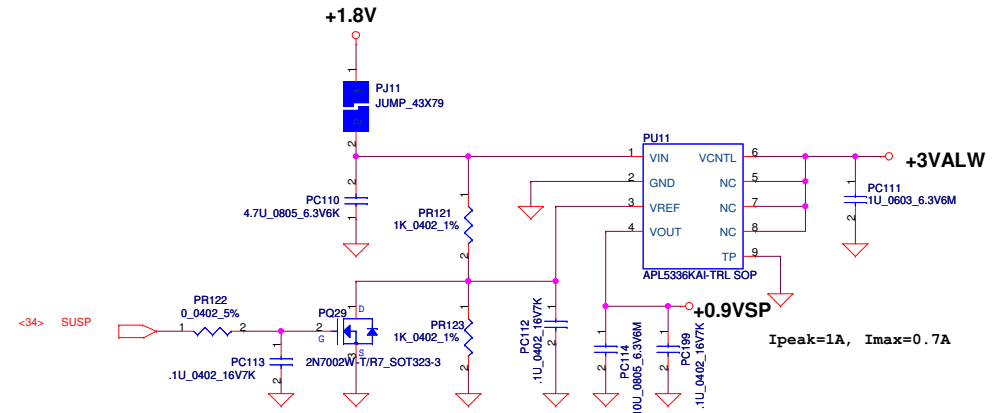
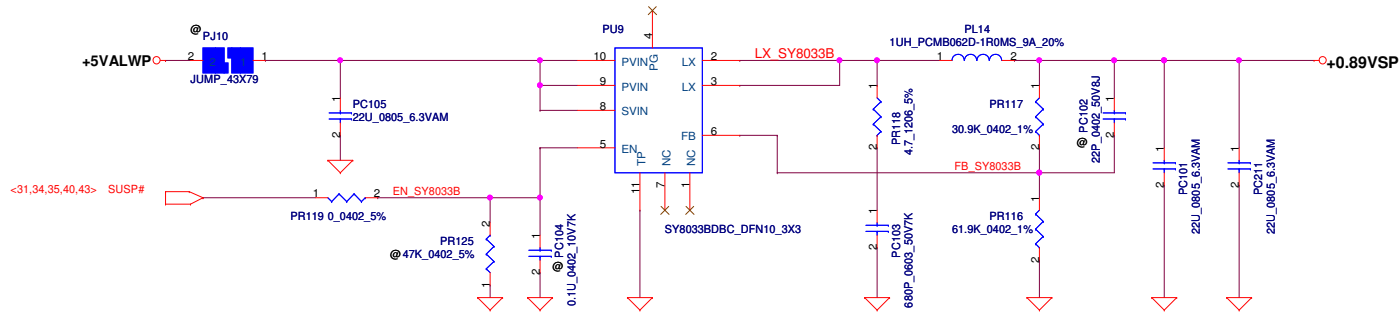
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2009/10/09		Deciphered Date		2010/10/09		Title	
										3V/5V	
										NAVD0 LA-6091P	
										Rev 1.0	
										Date: Wednesday, March 03, 2010	
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Size	Custom	Document Number	NAVD0 LA-6091P	Rev	1.0
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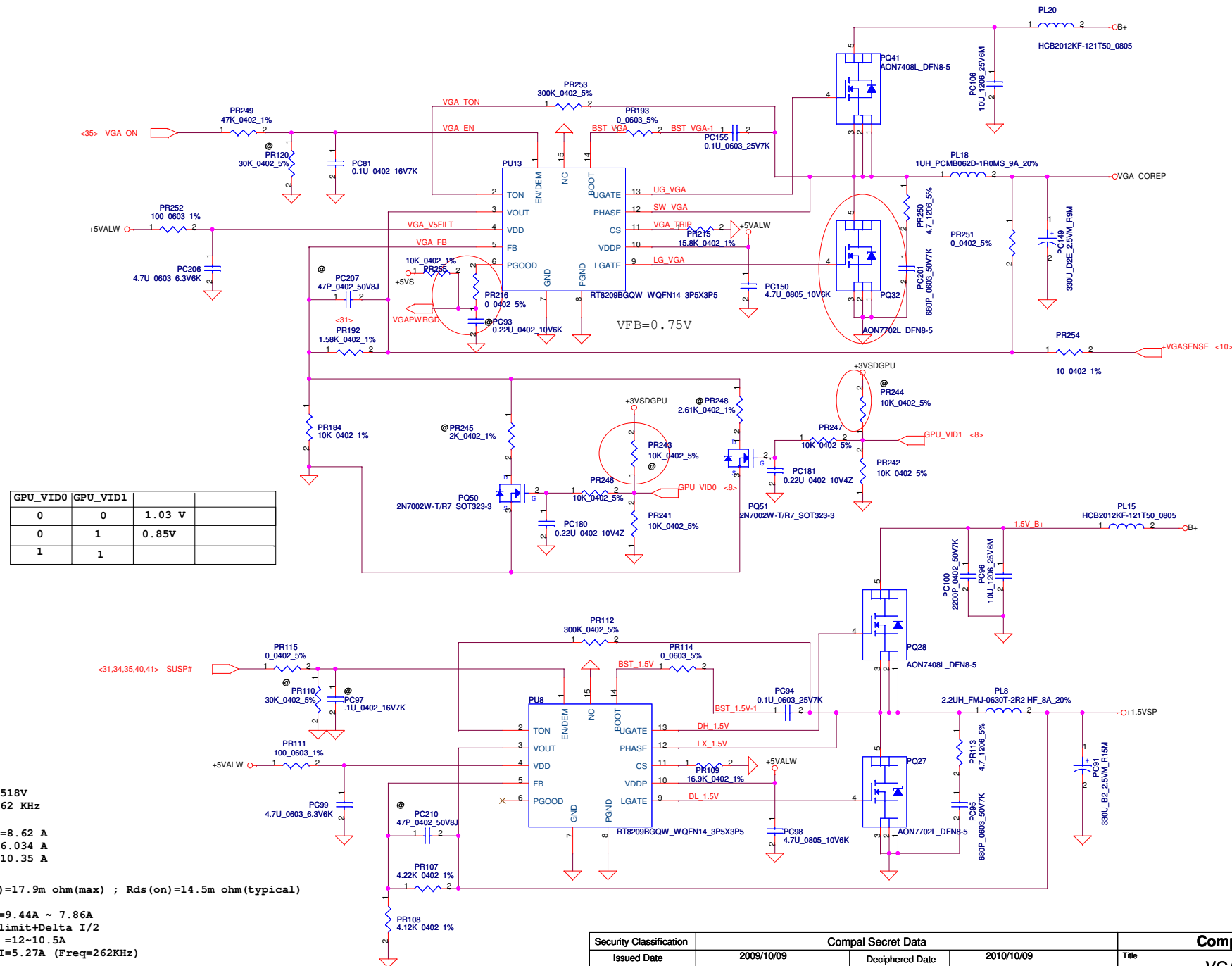
<Vo=0.89V> VFB=0.6V
Vo=VFB*(1+PR117/PR116)=0.6*(1+30.1K/61.9K)=0.8917V

Ipeak=2.64A



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delta I=3.27A 1/2 delta I=1.636 A
Iocp=RTEIP*ITRIP/RDS(ON)+1/2 I=14~11.98 A
Rds(on)=11~14m



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				Custom	1.0
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Version change list (P.I.R. List)

Page 1 of 1 for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		For save layout space and shortage	A		change PC50 PC53 to 0805 4.7u		
2		For VGA_core 51117 power good delay	A		Reserve PR216 PC93		
3		Save layout space	A		Delet PC35 PC36, change PC29 PC32 to 1206 10uF		
4		For cost down	A		change 0.89V from MP2121 to SY8033		
5		For cost down	A		delet Vin detector,battery OVP circuit		
6		For cost down	A		change 3V/5v from ISL6237 to TP551125		
7		For Design change	A		change PR116 to 61.9K PR117 to 30.1K PL14 to 1uH		
8		For cost down	A		change 1.5V PL8 to 3mm height		
9		For cost down	A		change VCCP PL7 to 3mm height		
10		For Design change	A		change PQ31 to IRFH3707		
11		For Design change	A		change PQ23 PQ25 PQ28 PQ30 TO AON7408		
12		change 1.5V enable RC ,for HW request	A		change PR115 to 0 ohm ,unpop PR101		
13		change VCCP enable RC ,for HW request	A		change PR99 to 1k ohm ,pc86 to 0.1u,unpop PR110		
14		change VGACORE enable RC ,for HW request	A		change PR249 to 47k ohm ,pc81 to 0.1u,unpop PR120		
15		For charger ripple			Add PC71 4.7u 0805 25V		
16		For charger ripple			change PL5 to 10uF		
17		Buyer suggest			change PQ36 from 2N7002 TO SSM3K7002FU		
18		Fix VGA_VID at 0.85V			delete PR248 PR245 ,change PR192 to 1.58K		
19		OTP INPUT PULL HIGH resister			Add PR29		
20		change OTP set			change PR31 to 13K		
21		1.8V enable cap			Add PC77 1u 6.3v X5R		
22		51125 VL cap size up to 1206			change PC205 to 1206 size		
23		Buyer suggest			change PC96 PC106 PC107 from X6S to X5R		

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				Size Custom	Document Number NAVD0 LA-6091P
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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1						2009.6.30	EVT
2						2009.6.30	EVT
3						2009.7.2	EVT
4						2009.8.4	EVT
5						2009.8.12	EVT
6						2009.8.12	EVT
7						2009.8.12	EVT
8						2009.8.12	EVT
9						2009.8.24	EVT
10						2009.8.24	EVT
11						2009.8.24	EVT
12						2009.8.24	EVT
13						2009.8.24	EVT
14						2009.8.24	EVT
15						2009.8.27	EVT
16						2009.9.4	DVT
17						2009.9.10	DVT
18						2009.9.30	PVT
19							
20							
21							
22							
23							

<2009/4/28>
Update new power schematic,
release first version NAV50 schematic

<2009/04/29>
. Add R1182 R1183 L3 on page 9
. Change J3 to R1184 on page 13

<2009/04/30>
. Change JDIM1 to SP07F001720 on page 7
. Del SATA1 Port on page 12
. Change R51 R57 R70 R63 R317 R314 R190 to 0402 Size on page 21

<2009/05/04>
. Add WWAN_CLKREQ# and R107 pull-high to +3VS on page 8
. Add CRT_DET# on page 10
. Add CRT_DET# circuit on page 13
. Add 3 LEDS on page 16
. Add BT/BTN Board CONN. on page 16
. Update TP/B CONN. to SP01000LB00 on page 19

<2009/05/11>
. Add INVT_PWM on Page 5
. Del R323 on page 5
. C74 change to 2.2U_0603 on page 6
. C267 change to 22U on page 6
. C391 change to 0.1U on page 6
. Del C67 C35 C33 C36 on page 6
. Del +LGI_VID and U71.A21 direct connect to +VCCP on page 6
. Follow Intel checklist, add R52 on FSB on page 8
. Add D5 D7 D8 on page 4
. Add R174 on page 9
. Add PCI_RST# on page 11
. Add C1115 C1114 C1116 C1117 C1118 on page 15

<2009/05/12>
. Follow Intel Layout Checklist, Add C141 on VDDSPD on page 7
. Modify SRC CLK PORT LIST on page 8
. Del CLKREQ_LAN# on page 8
. Change PCIE Port list on page 13
. Change USB Port list on page 13
. Add W/L 3G SW on page 16
. Del R103 on page 18

<2009/05/13>
. Change JMINI1 to PCIE Port 3 on page 15

<2009/05/14>
. Page8 Change C174 C175 to 10U_0603

<2009/05/14>
. Update New Power schematic
. Del R376 R377 on page 8
. Del D5 D7 D8 on page 4
. Change JLVDS1 to SP010006810 on page 9
. Add D6 for EMI on page 9
. Change C1106 to C_0603 type on page 9
. Change USB_OC# on page 13
. Add USB Port2 on page 20
. Change JP11 Pin define & Add D22 on page 19
. Change C512 to 1u_0402 on page 15
. Add U29 (MEDIA_LED#) on page 16

<2009/05/19>
.Update new clock GEN co-lay schematic on page 8

<2009/06/05>
.Update new clock GEN co-lay schematic on page 8
.Follow Intel check list change C161 C165 to 27P on page 8
.Follow Intel check list change C56 to 22uF on page 6

<2009/06/08>
.Update New Power schematic 06/06 version
Page 13- a.Del R203 (pull-up GPIO6 Resister)
b.Change R1184 NU
Page 17- a. Add VGATE
b. Del R1294
c. Change D30 NU
d. Change R1295 to 0 ohm
e. Add R1309 0 ohm on EC_RSMRST#
f. Pull-up LAN_WAKE# +3VALW
g. ICH_POK change to PCH_POK
h. Pull-up KB_RST# to +3VS
Page 10- a. Add R1283 R1284 ,Change R247 R249 to 10 ohm
b. Add @ on U10 U11 C301 C298
c. Del C302 C300 R1281 R1287

<2009/06/10>
. Page 7- Add C116 @
. Page 22- Modify USB_OC#1_2 to USB_OC#2
. Page 17- Modify PLTRST# to PCI_RST#
. Page 17- Add @ on R1311

<2009/06/12>
. Page4 Add C314 C313 C1150 D19 on +VCC_FAN1
. Page8 Add C1145 C1146 C1147
. Page10 Move CRT_DET# from Page13 to Page10
. Page13 Add +RTCVCC circuit

<2009/06/15>
. Update New Power schematic (change PBJ1 to PJP3)
. Page 10 modify C310 C308 C303 C307 C306 C304 Bom Structure
. Page 22 Modify Hole location by (ME drawing 06/12)

<2009/06/16>
. Page7 Modify DDR Command Control Pin pull-high Resister location
. Page9 Change R577 to 0402 type

<2009/06/17>
. Update New Power schematic 06/17
. Page9 modify LVDS Conn. Pin define
. Page9 Del C1110
. Page4 Add EMI solution D38 D39 D40

<2009/06/18>
. Update New Power schematic 06/18
. Page8 modify U4 Pin define and Q31
. Page13 Add R1376, R1377
. Page15 Modify C403
. Page23 Modify H11

<2009/06/19>
. Page4 Add new signal CPU_ITP , CPU_ITP#
. Page5 ADD R1378
. Page6 ADD C1152,C1153,C1154 C1160,C1161,C1162
. Page7 DDR_A_D8與DDR_A_D9互換
. Page8 ADD R1379,R1380,U77,R1381,C1157,R1382,R1383,R1384,C1157
. Page8 DEL C390
. Page9 ADD C1156
. Page11 DEL R1322, R1154
. Page13 DEL U77, ADD C1158
. Page17 ADD C1159

<2009/06/22>
. Page22 change IO Conn. pin34 from 48M to USB_ON#
. Page10 change JCRT1 P/N to SP010906182

<2009/06/23>
. Page15 Add C1163 C1164 C1165 C1166
. Page18 change PWR/B Conn. P/N to SP01000H300
. Page22 change JUSB1 JUSB2 P/N

<2009/06/24>
. Page8 Change C1350 C1351 to 0402 type
. Page10 Add R1385 R1386 on JVGA_HS JVGA_VS

<2009/06/25>
. Page22 move some parts to I/O Board , Add the MONO_IN_R on M/B

<2009/06/29>
. Page16 Change JP24 to ACES_88266_05001
. Page15 Change JMINI1 to FOX_AS0B246-S50U-7F_52P-T

<2009/06/30>
. Page18 Change PWR_LED# to PWR_PWM_LED#
. Page17 Add PWR LED DETECT PIN on Pin97

<2009/07/02>
. Update New Power schematic 07/02
. Page9 Add C1167 C1168 for RF request.
. Page13 Change R223 to 100K
. Page16 change JP24 to ACES_85201-0505N
. Page17 Del R1387 R1388 on EC Pin97
. Page17 Add New Board ID to separate NAV50 NAV60
. Page17 Change 展頻IC to SA00003J400 (New)
. Page18 Add D41 for ESD

<2009/07/03>
. Page18 Add D41.2 to PWR_PWM_LED#
. Page8 Change co-lay net name to +1.5VM_CK505
. Page20 Change JP2 Pin42 to +5VS

<2009/07/06>
. Page18 Add pwr switch for NAV50

<2009/07/08>
. Page5 Add 470pf on H_SMI# for known issue.

<DVT START>

<2009/08/04>
. Page5 CLK_CPU_HPLCLK CLK_CPU_HPLCLK# exchange
. Page9 Change JLVDS1 to P/N ACES 88341-3001 30P
. Page17 del PM_1.8V(U6.82) ,Del R1310 R1311
. Page18 Del D41

<2009/09/03>
. Page7 Change C112 to 0402 type
. Page8 Add T6 on CLK_48M_CR
. Page16 Modify JP18 Pin define change +5VALW +5VS to +3VALW +3VS
. Page20 Change Pin 18, 23 to +1.5VS change Pin7 , 9 to USB20_P7 N7
. Page21 Del H12

<2009/09/08>
Update Power schematic 0904
. Page18 Change R1388 to 100 ohm 0402
. Page18 Change LED1 to SC591NB5A00

<2009/09/10>
Update Power schematic 0910
. Page22 unmount Q6 Q8

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